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# NOVEL HIGH-PASS FILTERING METHOD REJECTS NOISE WHILE PRESERVING INTER-CHANNEL PHASE MATCH

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### 1. INTRODUCTION

Signals contaminated by low frequency noise can be high-pass filtered to remove noise and any DC component, with the result that a wider signal dynamic range may be preserved through the input signal amplifier path than would be possible with unfiltered signals. However, phase matching of a multiplicity of high-pass filtered amplifier chains is difficult to maintain with traditional techniques, though very important to measurements such as sound intensity or phased array processing. One recently adopted international sound intensity standard, IEC 1043 [1], is specifically concerned with measurement accuracy of both the two-microphone intensity probe and the related processing of the signals by an intensity analyzer. Measurements of the highest quality are possible only when very close phase match exists between the measurement channels. The phase match is particularly an issue for frequencies below 100 Hz, where the wavelength of sound is long relative to the spacing between microphones. To meet the Class 1 measurement quality standard of IEC 1043, all elements of the instrument (including probe and measurement channel) must collaborate to result in phase differences between channels on the order of 0.08 degrees below 200 Hz. The standard draws a distinction between required accuracy of an analyzer independent of the probe. For the analyzer, the cross-channel phase match must be less than 0.017 degrees.

At low frequencies, the phase match between measurement channels is primarily affected by differences in the mechanical construction of the individual microphone capsules. Other sources of mismatch include preamplifiers, input signal conditioning including high-pass filters, broadband weighting filters, gain stages, and protection circuitry. Even if high-pass filters are not required to block low-frequency rumble signals from saturation of the ADC (and preceding analog stages), a DC blocking

capacitor is normally used in the input stages to eliminate offset voltages as present at the microphone preamplifier output.

Quality high-pass filters are expensive and suffer from phase errors due to component tolerances and differences in temperature coefficients per channel. For example, in a simple blocking-capacitor filter, a mere 1% error in the capacitor value causes nearly 0.3 degrees phase error at the filter cutoff frequency. Usually only one or two specific corner frequencies are available (with a fixed filter shape, e.g., Butterworth), tuned to the acoustic measurement of interest. Simple AC coupling circuits have comer frequencies around 1 Hz or less, while a measurement over audio frequencies may include a 20 Hz high-pass filter. The HP E1432A 16-channel VXI digitizer, for example, includes an AC coupling circuit, which is the primary factor in the low frequency worst case cross-channel phase match of 0.2 degrees from 50 Hz to 200 Hz [2].

Various methods have been employed to calibrate and correct the measurement system so that accurate intensity measurements can be performed [3]. In addition, phase matched microphones benefitting from improvements in design and manufacturing techniques have been brought to market [4]. This paper focuses on a technique for marked improvement of the analyzer's AC-coupled cross-channel phase performance, even when high-pass filters are included in the input path. The goal of this effort is the elimination of a phase correction step, so that the basic uncorrected hardware specifications of the intensity system are adequate for the highest quality intensity measurements.

## 2. DSP CONTROLLED ANALOG REJECTION

A new approach to maintaining accurate phase match between high-pass filtered signals, even near the filter cutoff frequency, combines traditional analog filtering and modern digital signal processing techniques. A block diagram of the new front-end architecture is shown in Fig. 1.

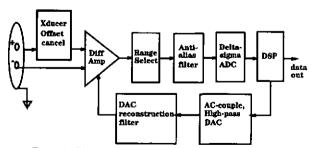


Figure 1. Block diagram of the new input architecture

Except for the feedback path through a 20-bit digital-to-analog converter, the topology is fairly typical of an audio bandwidth input section, including

digital filtering implemented on the digital signal processor (DSP), where performance is limited only by the stability of the sampling clock and the digital precision to which variables and coefficients can be represented. However, if filtering were done only within the DSP, the analog signal path would have to accommodate the entire input signal, including DC offsets and low frequency AC signals which are to be removed in the high pass filter. By including the analog feedback path from the DSP, these unwanted signals are removed early in the signal path and dynamic range is maximized. The resultant high-pass filter comprises both the DSP algorithm and the analog feedback path (including DAC and ground reference on the differential amplifier), and is easily commanded to any cutoff frequency (with milli-Hertz resolution).

The HP E1433A 8-channel VXI digitizer front-end embodies the new architecture. Any high-pass filter corner frequency between 1 Hz and 100 Hz may be selected per channel, each of which has a 12 dB per octave transition band. The worst case cross-channel phase match for this product is 0.015 degrees from 50 Hz to 200 Hz [5], even at the corner frequencies of the high-pass filters. Although the research describes a second-order filter with Butterworth (maximally flat magnitude) characteristics, the techniques are applicable to filters of higher order and which have other characteristics. For example, the lower transition band of an A-weight filter may be implemented in a similar fashion.

## 3. FILTER TOPOLOGY

A common characteristic of feedback filters is a memory of past events. In analog systems, this typically takes the form of one or more capacitors. In a digital system, there are delay elements, often embedded in a DSP algorithm. These memory elements are key to setting the response of the system. In the hybrid filter, both the DSP and the analog signal path have memory. In the DSP, memory is built into the feedback algorithm, but in the analog path, it is present in elements such as the DAC reconstruction filter and in the delay introduced by the sigma-delta ADC architecture. Because changes in the analog signal path will have a direct effect on the overall filter response, it is important to keep that path as stable as possible within the constraints of other performance issues. To that end, the DAC reconstruction filter cutoff frequency is set far above the maximum AC filter cutoff frequency.

The ADC delay is a result not of analog components but of an FIR digital filter embedded in the ADC, and as such it is essentially as stable as the crystal-controlled clock which drives both the ADC and the DSP. In spite of this significant delay in the ADC, DSP algorithms implement most of the memory in the system described here, and because of that, they most strongly influence the overall filter performance. In turn, those algorithms

are very stable and accurate because of the crystal-controlled clock and 24-bit DSP word length.

Fig. 2 shows the topology of the filter, including its feedback and the DSP filtering algorithm. This diagram relates closely to Fig. 1, with the analog signal path and DAC and ADC replaced by z-domain representations of their transfer functions, and the DSP filtering algorithm shown in detail. One analog element of the system not modeled is the analog DAC reconstruction filter. It is assumed to have a small delay in the frequency range of interest.

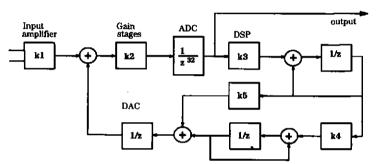


Fig. 2. Filter processsing topology including analog sections

Standard feedback analysis techniques can be used to derive the following z-domain transfer function for the system diagrammed in Fig. 2:

Equation 1 tells us several things about the filter, even without having put

$$g(z) = \frac{k_1 \cdot z^{32} \cdot (z-1)^2}{z^{35} - 2 \cdot z^{34} + z^{33} - k_2 \cdot k_3 \cdot k_5 \cdot z + k_2 \cdot k_3 \cdot k_5 - k_2 \cdot k_3 \cdot k_4}$$
(1)

in specific values for the various coefficients. First, the filter has a 32nd order zero at z=0: this simply represents the delay of the ADC and has no effect on the filter frequency response. Second, there is a second order zero at z=1. This is exactly the desired case for a second order high pass filter, and does not depend on the values we choose for the coefficients. Finally, the 35th order denominator implies a system with 35 poles, and since we have only three independent coefficients to adjust (k1 not appearing, and k2 and k3 always appearing as a product), we cannot control the position of all the poles independently. In fact, what we find is that it is fairly straightforward to select coefficients to place two of the poles at exactly the positions required to implement common characteristics, such as Butterworth. So long as that is done for a sufficiently low filter cutoff frequency, the remaining 33 poles fall well within the z-plane unit circle, implying feedback loop stability. However, those

poles do affect the filter frequency response, and something further must

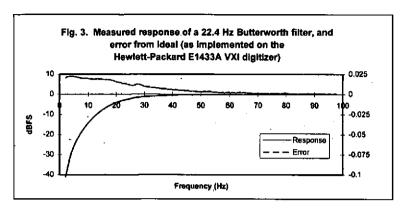
be done to correct the filter so that the overall response is the desired one, e.g., a Butterworth shape. It is worth noting that the 33 unwanted poles come directly from unwanted delays (memory) in the closed control loop which is the filter. It would be possible to bypass the unwanted delay by simply closing the feedback loop completely within the DSP, a wholly digital path. However, then the advantage of removing the undesired signal early in the analog path, with resultant increased dynamic range, would be lost.

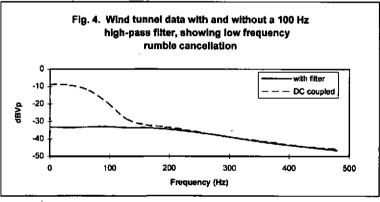
The positions of the unwanted poles are known accurately from analysis of the overall feedback loop. It is thus possible to compensate for them. Since the desired high-pass filter is implemented with two poles and two zeros which have already been accurately placed, it is only necessary to cancel the unwanted 33 poles with zeros. An FIR digital filter has only zeros, and these zeros can be placed easily at the same positions as the unwanted poles. The overall filter implemented in the HP E1433A, then, consists of a feedback filter whose characteristics are determined mainly by, and controlled accurately by, a DSP algorithm, but which includes an analog feedback path to maximize channel dynamic range, followed by an FIR filter implemented in the same DSP. The result is a very accurate, compact filter which is easy to adjust in cutoff frequency.

### 4. RESULT

Just what performance is achieved in an actual implementation of the filter described above? Are there limits to the performance that aren't apparent from the mathematical analysis of the system? To answer these questions, we have run tests on the filter to measure filter accuracy. channel-to-channel phase match, overload characteristics, and other parameters. The filter transfer function of Fig. 3 shows the measured 12 dB/octave stoppand attenuation and flat passband characteristic of a 22.4 Hz Butterworth filter (left scale), and its error from the ideal Butterworth response (right scale). Note the very small differences between the measured and ideal responses. The results are typical for a randomly selected channel. With a calibration only for the filter control loop gain, cross-channel phase matching is always within 0.015 degrees, even at the filter cutoff frequency, and is typically 0.007 degrees. Finally, Fig. 4 shows sound pressure level spectra from a wind tunnel test in which there was significant low frequency noise that was not of interest in the measurement. The spectrum with significant content below 100Hz is DC coupled, and the other spectrum is AC coupled with a 100Hz high pass cutoff frequency. Each spectrum was taken at the most sensitive input range possible before overload occurred; the DC coupled spectrum was taken on an 0.5 volt full scale input range, and the AC coupled on a 0.1 volt range, resulting in 14 dB greater dynamic range for the signals of interest.

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# 5. REFERENCES

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