Proceedings of the Institutue of Acoustics

HIGH EFFICIENCY WAVE TRANSLATION FILTERS FOR SONAR BAND SELECTION

A. G. Constantinides (1) and T. E. Curtis (2)

(1) Imperial College of Science and Technology, London
(2) Admiralty Research Establishment, Portland

1. INTRODUCTION

High performance filtering algorithms are needed in many signal processing applications: typical requirements are for interpolation and decimation filters for sample rate alteration and for analysis band selection. Digital wave filters [1] are attractive in these applications since they are digital implementations of doubly terminated loss-less ladder networks and maintain the advantages of low coefficient sensitivity and ease of design of such structures. Additionally circuits with very low arithmetic complexity, typically requiring only one or two multiplications per input data sample, can be developed by constraining the ratio of the filter cut-off frequency to the clock rate. The resulting structures can be implemented effectively in either "off-the-shelf" DSP components or high performance ASICs: they have found practical applications primarily for complex hetrodyning and decimation of beam data prior to spectral processing but are also useful in other areas.

2. GENERAL REQUIREMENTS AND FILTER DEVELOPMENT.

Band definition and filtering operations represent a major processing load in passive sonar systems. Typically the band selection function is used to define analysis bands for further processing after beamforming: it is also convenient at this stage in the processing chain to generate complex data so that down-stream spectral processes can be implemented more efficiently. Consequently the band definition circuits usually include complex hetrodyning, pre-multiplying the real beam data samples by a complex exponent representing the band-shifting frequency, with the resulting phase and quadrature data feeding to a pair of low-pass filters - see Figure 1. The filter outputs are then decimated to reduce the data rate to that commensurate with the analysis bandwidth.

In most systems, large numbers of beams need to be processed together and many analysis bands are required on the same beam data to allow, for example, surveillance, vernier and tracking analysis bands to be processed simultaneously. In large aperture array systems generating several hundred beams, this results in high processing loads, with maybe several thousand filters, each individually selectable in terms of bandwidth and centre frequency, realised simultaneously.

Efficient interpolation and decimation processes are also useful in other areas: for example, for bandwidth reduction immediately after channel digitisation (thus allowing simple, low-cost analogue anti-alias filters to be used), to reduce data rates for transmission, for example up tow cables, for interpolation to reduce the effects of time delay quantisation in time domain beamforming systems, for image data interpolation to reduce contouring on displays, etc.

In many current systems, these filtering functions are provided using either finite impulse response or recursive digital filtering schemes [2]. For high throughput systems, recursive filters are needed to reduce the overall computational load but for a typical realisation, using parallel bi-quadratic sections such as the system show in Figure 2, the cost of each filter, in terms of arithmetic complexity, is high - eight multiplications per input data sample, for the 8th order system shown.

The system performance obtained of this type of filter is only marginally acceptable: typically 50 dB out of band rejection, 1 dB in band ripple and normalised transition bandwidths of 0.25 can be achieved.

The following paragraphs outline the development of a simple hardware structure for filtering which produces higher performance with significantly lower hardware complexity. It can be used for interpolation and decimation with arbitrary sample rate alteration factors but the following paragraphs concentrate on interpolation and decimation by factors equal to powers of two, (realised by cascading sections each interpolating or decimating by two). These implementations have proved to be the most useful in practical applications and provide some compact hardware realisations.

The method for the filter development follows that of Valenzuela and Constantinides, detailed in Reference 3.

2.1(a) Basic Filter Transfer Function.

The complexity of the implementation shown in Figure 2 arises because the filtering operations are performed at the input data rate: the filter output data is decimated to reduce the final output rate only after most of the filtering processes have been carried out. A reduction in complexity would be possible if the data could be decimated prior to processing, with the filtering operations performed at the output data rate. This requires the development of a filter synthesis method where the processing is performed at minimum data rates, rather than the more conventional filter design approach that involves re-arrangement of some prototype transfer function operating on data at the filter input rate.

One way to achieve this minimum data rate operation is shown schematically in Figure 3(a): an N-fold reduction is obtained by feeding input data samples sequentially into N sub-filters with the output calculated by summing the appropriately delayed outputs from all sub-filters. Interpolation is obtained in a similar way - Figure 3(b).

The transfer function of the system shown in Figure 3(a) is given by:-

$$(1) \qquad H(z^{-1}) = \sum_{i=0}^{N-1} z^{-i}.H_i(z^{-N})$$

If the sub-filter is an all-pass network with a transfer function expressed as:-

$$(2) \qquad H_i(z^{-N}) = \prod_{k=1}^{K_i} A_{i,k}(z^{-N})$$

where

$$A_{i,k}(z^{-N}) = \frac{a_{i,k} + z^{-N}}{1 + a_{i,k}.z^{-N}}$$

then substituting equation (2) into (1) gives the overall transfer function of the parallel network:-

$$(3) \qquad H(z^{-1}) = \sum_{i=0}^{N-1} z^{-i} \prod_{k=1}^{K_i} \frac{a_{i,k} + z^{-N}}{1 + a_{i,k}.z^{-N}}$$

The frequency response of the network can be calculated by evaluating equation (3) on the unit circle:-

$$A_{i,k}(\omega) = \exp\{j\Theta_{i,k}(N\omega)\}$$

$$= \frac{a_{i,k} + \exp\{-jN\omega\}}{1 + a_{i,k}.\exp\{-jN\omega\}}$$

Substituting

$$\exp\{-jN\omega\} = \frac{1 - j.\tan(N\omega/2)}{1 + j.\tan(N\omega/2)}$$

gives:-

$$\Theta_{i,k}(N\omega) = -2.\tan^{-1}\left[\frac{1 - a_{i,k}}{1 + a_{i,k}}\tan(N\omega/2)\right]$$

The required filtering function can then be synthesised if $\Theta_{i,k}(N\omega)$ is selected such that $H(\omega)$ approximates to one in the filter pass band and to zero in the stop band.

2.1(b) Interpolation/decimation by a Power of Two

Sample rate alteration by a power of two can be obtained by repeated interpolation/decimation using the simplified two branch structures in Figure 4. The general transfer function given by equation (3), evaluated for the two branch case, is:-

$$(4) \qquad H(z^{-1}) = \prod_{k=1}^{K_0} \frac{a_{0,k} + z^{-2}}{1 + a_{0,k}.z^{-2}} + z^{-1}.\prod_{k=1}^{K_1} \frac{a_{1,k} + z^{-2}}{1 + a_{1,k}.z^{-2}}$$

Equation (4) represents a stable system if all coefficients are less than unity and Reference 3 shows that such structures simulate doubly terminated loss-less ladder networks. The frequency response of the network can be calculated by evaluating equation (4) on the unit circle, and we require to choose the filter coefficients $a_{i,k}$ so that:-

$$H(\omega) \rightarrow 1 \quad \text{for} \quad 0 < \omega < \pi/2 - \omega_t/2$$

$$H(\omega) \rightarrow 0 \quad \text{for} \quad \pi/2 > \omega > \pi/2 + \omega_t/2$$

where ω_t is the normalised transition bandwidth.

A number of design methods are available to achieve this; both non-linear optimisation techniques and classical analogue filter methods have been used for practical designs. Figure 5 plots the stop band attenuation and transition bandwidth that can be obtained for an optimised equi-ripple design versus coefficient values for the simplest networks (K_i=1 or 2). If better out of band attenuation or a sharper transition band is required, higher order all-pass sections can be used.

3. PRACTICAL FILTERS.

Figure 6(a) shows the calculated frequency response for a two-path design with $a_{0,1} = 0.1413$ and $a_{1,1} = 0.59$. The filter provides out of band rejection of -60 dB, negligible in-band ripple and a transition bandwidth of 0.24 and requires just **one multiplication per input data point.**

If the all-pass network outputs are subtracted rather than added, the complementary high-pass frequency response shown in Figure 6(b) is obtained.

Cascading sections as shown in Figure 7 allows narrower filter bandwidths to be realised: Figure 8 shows the response of a decimate-by-eight system, with a cascade of three identical fifth order sections (using the coefficient values in Figure 6). Filter sub-bands can be selected by adding or subtracting the all-pass branch outputs at each decimation stage as necessary.

This implementation uses just two coefficient values, and, since the data rate is halved on each successive stage of processing, only three multiplications are required every two input data points.

Better out of band attenuation and a sharper transition band is obtained using higher order all-pass sections. Figure 9 shows the response for a seventeenth order design (K_0, $K_1 = 4$): attenuation of 120 dB and a sharp transition bandwidth is obtained with eight multiplications per input data point (for a decimate-by-eight using repeated decimation-by-two).

A number of practical implementations of the basic all-pass section required for the interpolation/decimation scheme are shown schematically in Figure 10.

A hardware realisation of Figure 10(c), using "of-the-shelf" fast static RAM and bipolar multipliers, can handle input data at the rate of one input sample every 100 nSecs and, with an channel sample rate of 16 kHz, several hundred filter channels, with bandwidths and centre frequencies selectable individually, can be processed simultaneously.

Higher throughput and improved performance can be obtained using an ASIC design: Figure 11 shows a 24-bit gate array based implementation using the all-pass network topology shown in Figure 10(a). This device was developed in colaboration with GEC(Avionics), Rochester, and uses LSI Logic Ltd 9000 series 'sea-of-gates' technology. Four devices, together with local RAM storage and micro-coded controllers, fit on a standard PCB (double Euro card size). The board (Figure 12) allows filter order and decimation ratio to be selected on a channel-by-channel basis: it provides a total input bandwidth of around 80 mega-samples per second and realises in excess of four thousand fifth order filters with an input sample rate of 16 kHz per channel.

4. CONSTRAINED COEFFICIENT DESIGNS.

As only a small number of coefficient values are required for the filter system, an optimised structure can be developed to implement each efficiently. The intrinsic low coefficient sensitivity of the network permits filters with good performance to be designed using a canonic signed digit representation of the coefficients, with a limited number of non-zero digits, i.e. the coefficient scaling can be achieved using a simple shift/add/subtract scaling circuit.

As well as producing compact hardware implementations, this constrained coefficient canonic signed implementation is useful in software based systems. The shift/add structure shown in Figure 13 can be programmed efficiently in machine code and provides a useful interpolation algorithm to reduce contouring on sonar images. Figure 14 shows the raw data from a broad-band passive (P-Theta) system, together with data interpolated using this technique: the interpolated data provides a more acceptable picture for the operators, improved target bearing estimation and easier manual tracking.

High performance filters can be implemented with high throughput on small gate arrays or even EPLDs, using the schematic in Figure 15(a). Figure 15(b) shows the response from such a design; it uses a hard-wired shift/add/subtract network with just two binary shifts for coefficient scaling: out of band attenuation in excess of 60 dB attenuation is achieved in this way.

5. DISCUSSION.

A number of low-complexity, high performance filtering techniques, based on wave translation interpolators and decimators, have been outlined. These have allowed a number of practical filter implementations to be developed that are useful in a range of sonar applications.

By constraining one branch of the interpolator/decimator to be a straightforward time delay [4], structures with arbitrarily linear phase over the pass-band have also been designed [5]: these have been employed in a number of applications where their computational efficiency, compared with the more usual FIR linear phase interpolators, are a major advantage.

6. REFERENCES.

[1] see for example:
A. FETTWEIS, 'Wave Digital Filters with Reduced Number of Delays', J Circuit Theory and Applications, 2, 1974.
A. G. CONSTANTINIDES, 'Alternative Approach to the Design of Wave Digital

Filters', Electronics Letters, 10, 1974.

[2] see for example:
'DIGITAL FILTERS AND THEIR APPLICATIONS' by V. CAPPELLINI, A.G. CONSTANTINIDES and P. EMILIANI, published by Academic Press, 1978.

[3] R.A. VALENZUELA and A.G. CONSTANTINIDES: 'Digital Signal Processing Schemes for Efficient Interpolation and Decimation', IEE Proc Part G, 130, 1983.

[4] see for example:
M. RENFORS and T. SARAMAKI, 'Recursive Nth-band Digital Filters - Part I: Design and Properties', IEEE Trans CAS, 34,1987.
M. RENFORS and T. SARAMAKI, 'Recursive Nth-band Digital Filters - Part II: Design of Multistage Decimators and Interpolators', IEEE Trans CAS, 34,1987.

[5] S. B. BRUTON, 'The Design of Low Complexity Digital Filters for Decimation and Interpolation', MSc Thesis #RNEC-SP-88002, Royal Naval Engineering College, Manadon, Plymouth, 1988.

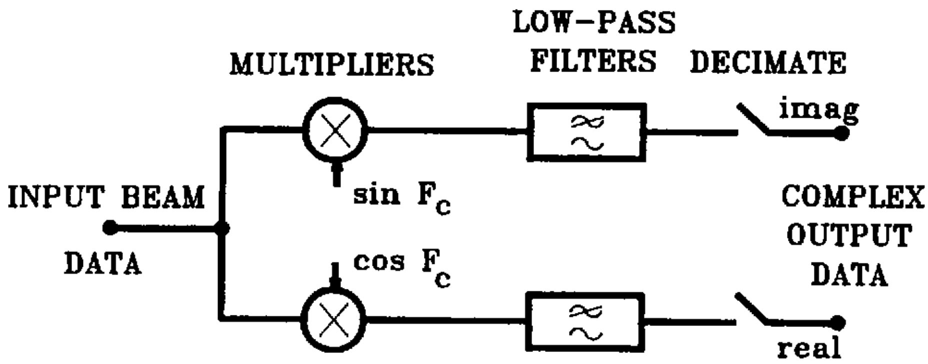


Figure 1 - Complex Hetrodyning Schematic

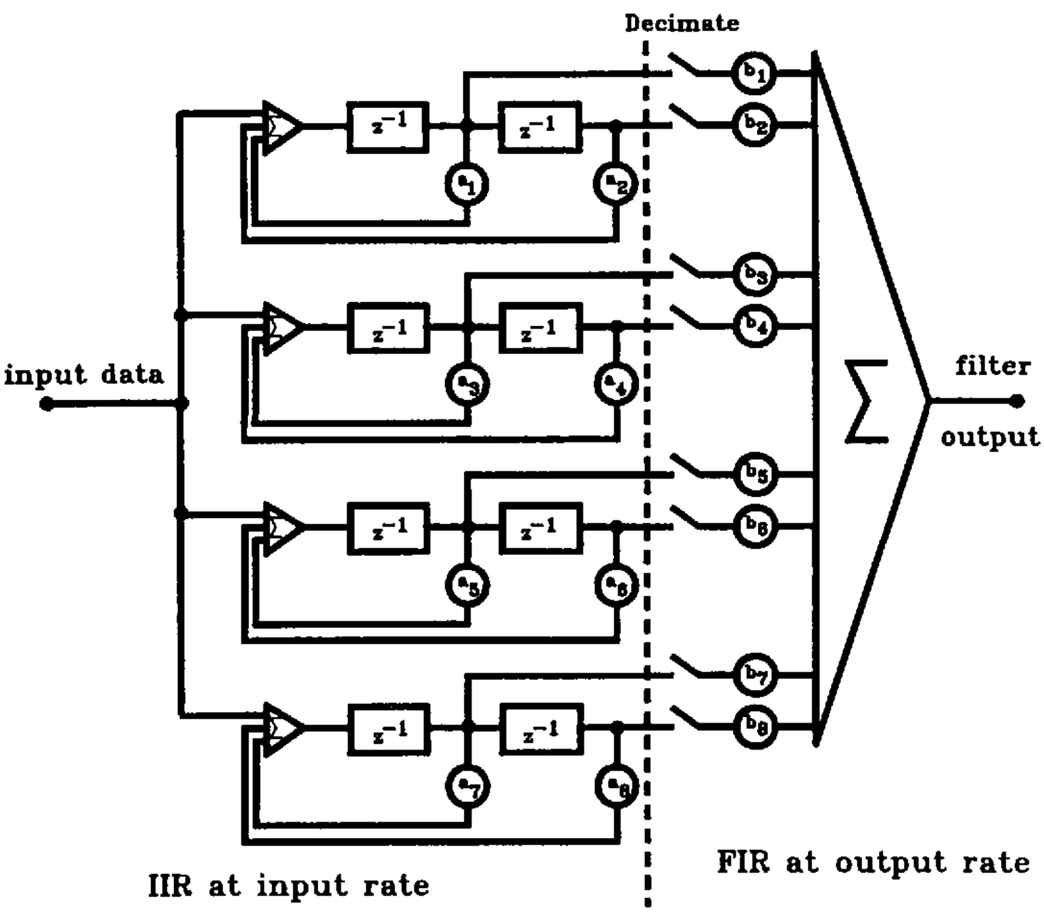


Figure 2 - Typical Eigth-order Parallel Bi-quad Schematic

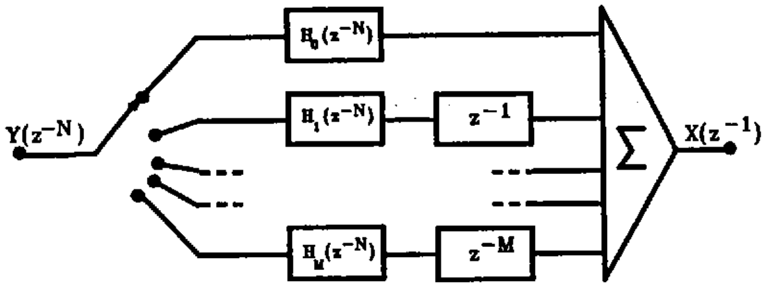


Figure 3(a) - Decimation by N

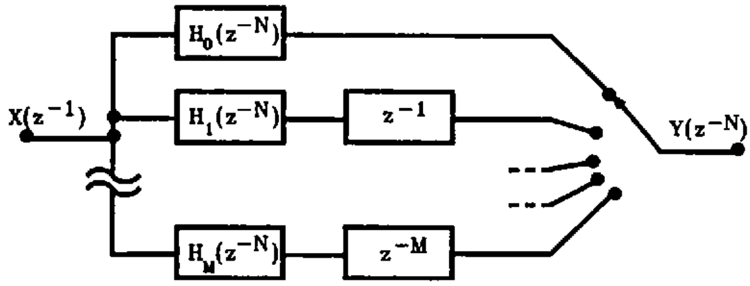


Figure 3(b) - Interpolation by N

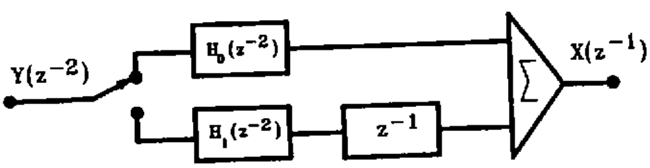


Figure 4(a) - Decimation by Two

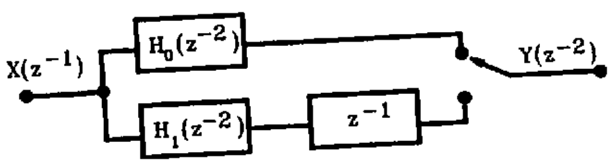
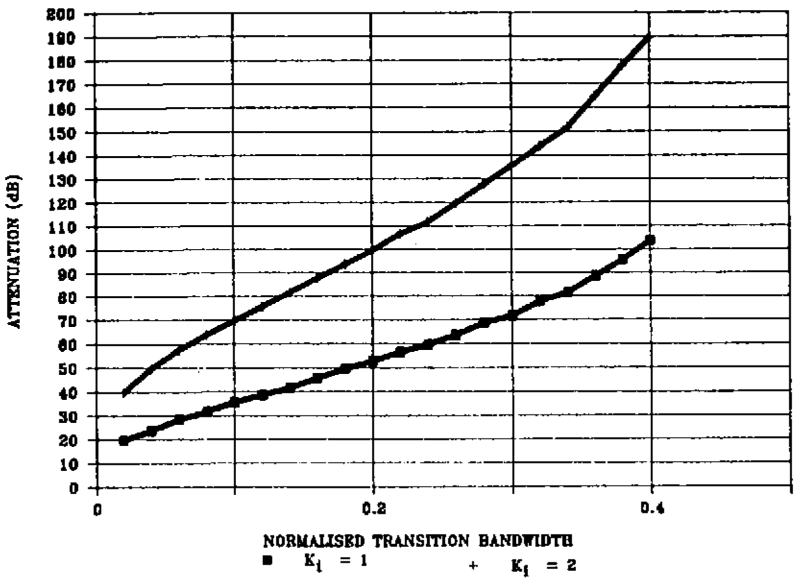


Figure 4(b) - Interpolation by Two

STOP BAND ATTENUATION VS TRANSITION BANDWIDTH



COEFFICIENT VALUES VS TRANSITION BANDWIDTH

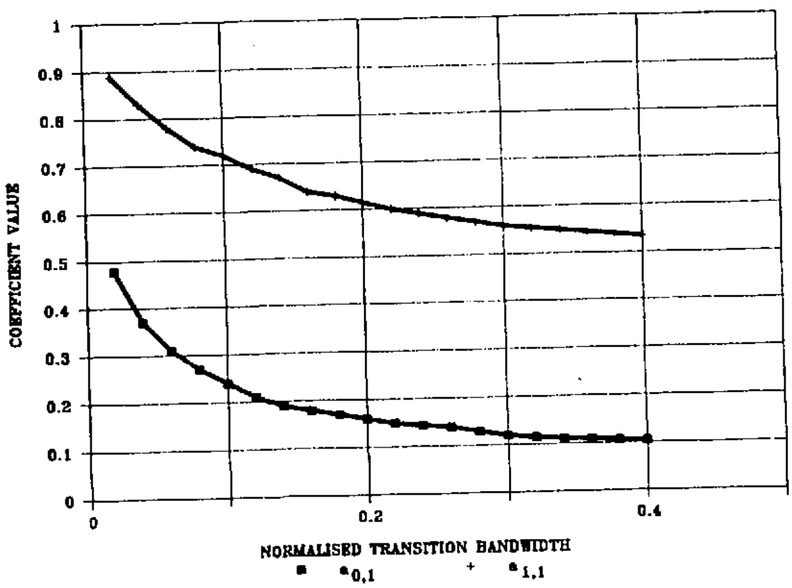


Figure 5 - Stop-band Attenuation and Transition Bandwidth vs Filter Coefficient Values

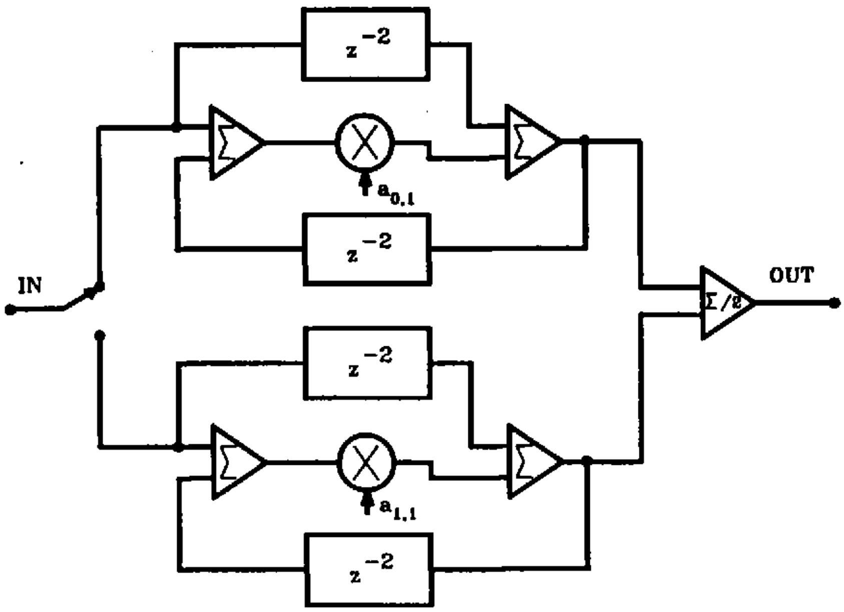
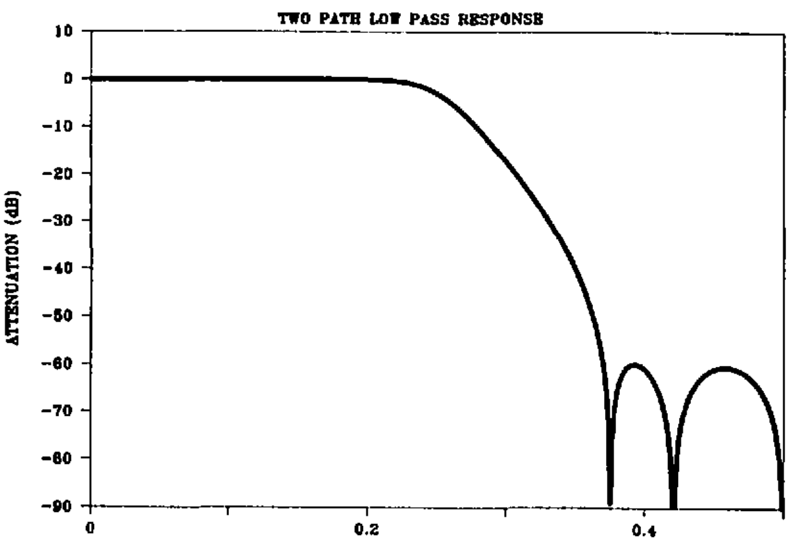


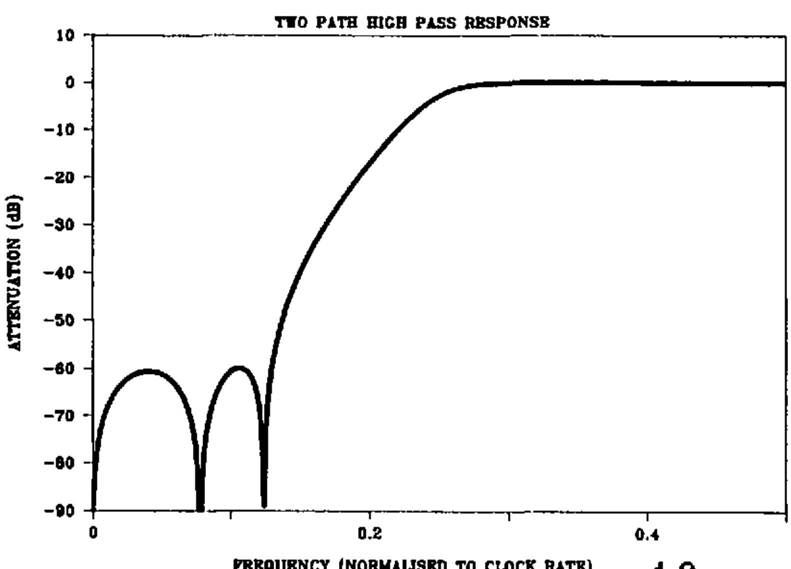
Figure 6

Two Path Decimator



(a)

Two Path Decimator
5th Order Low Pass Response



(b)

5th Order High Pass Response

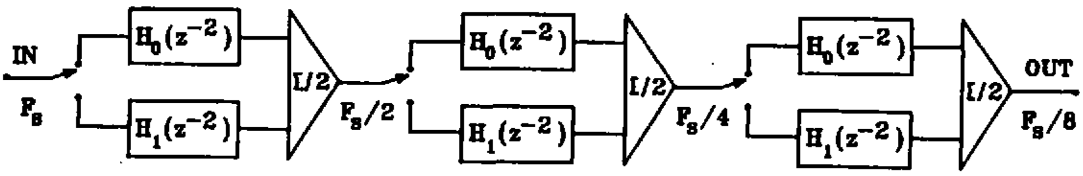


Figure 7 - Decimate by Eight Cascade

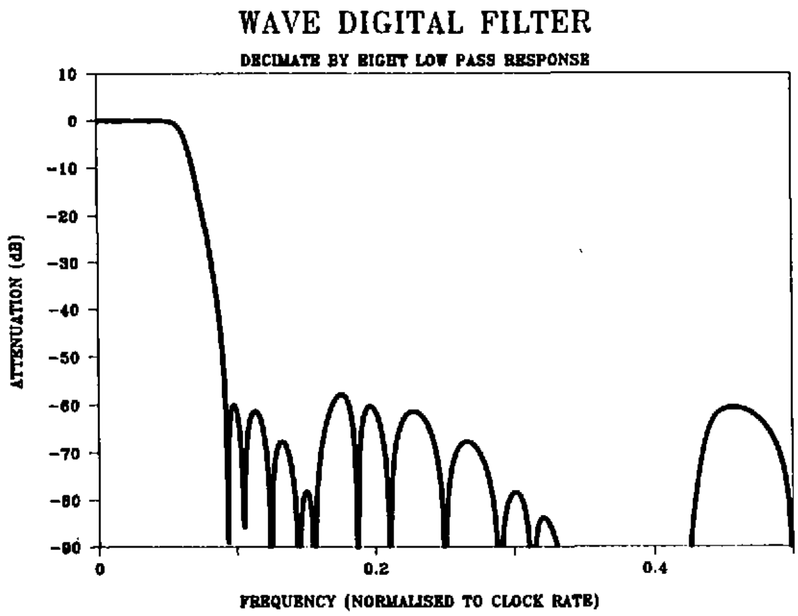


Figure 8

Response of Decimate by Eight System

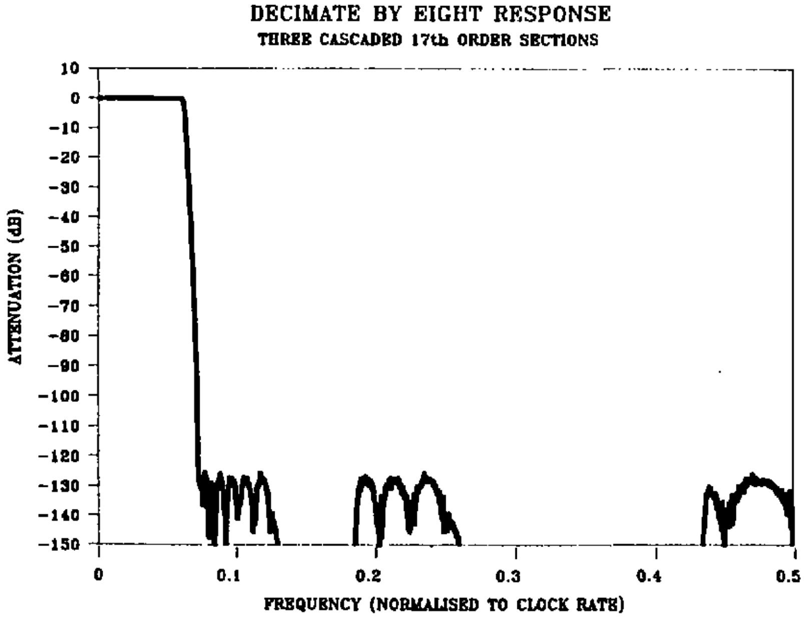


Figure 9

Two Path Decimator 17th Order Low Pass Response

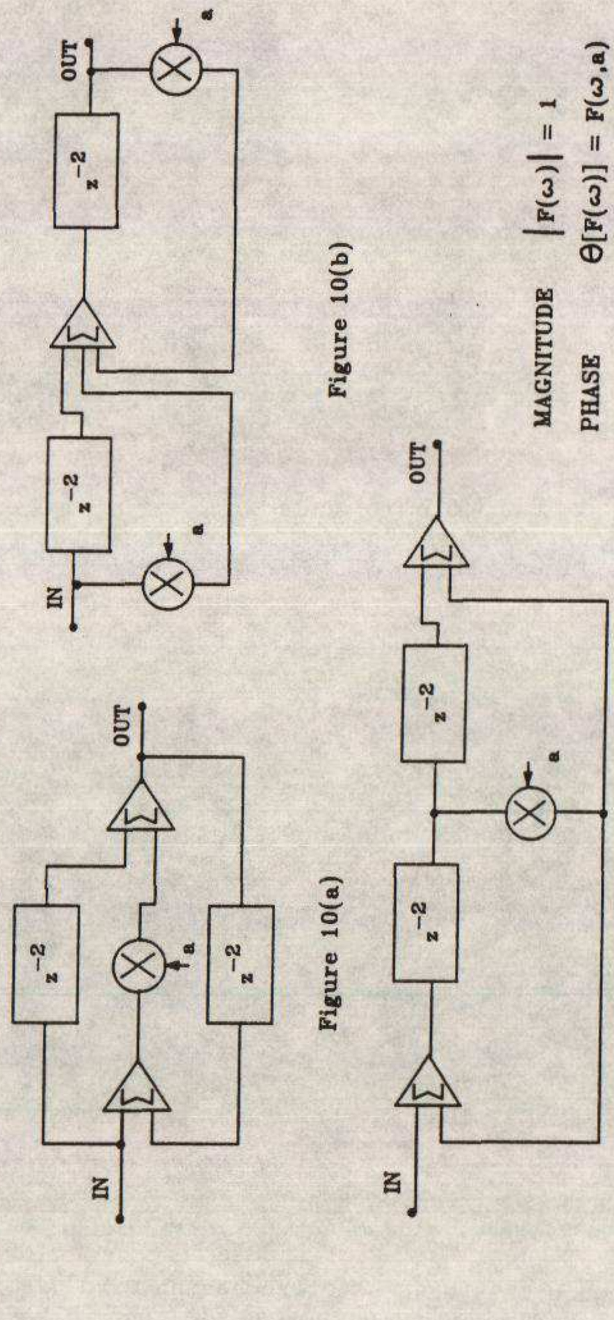


Figure 10 - All Pass Network Topologies

HIGH EFFICIENCY WAVE TRANSLATION FILTERS FOR SONAR BAND SELECTION

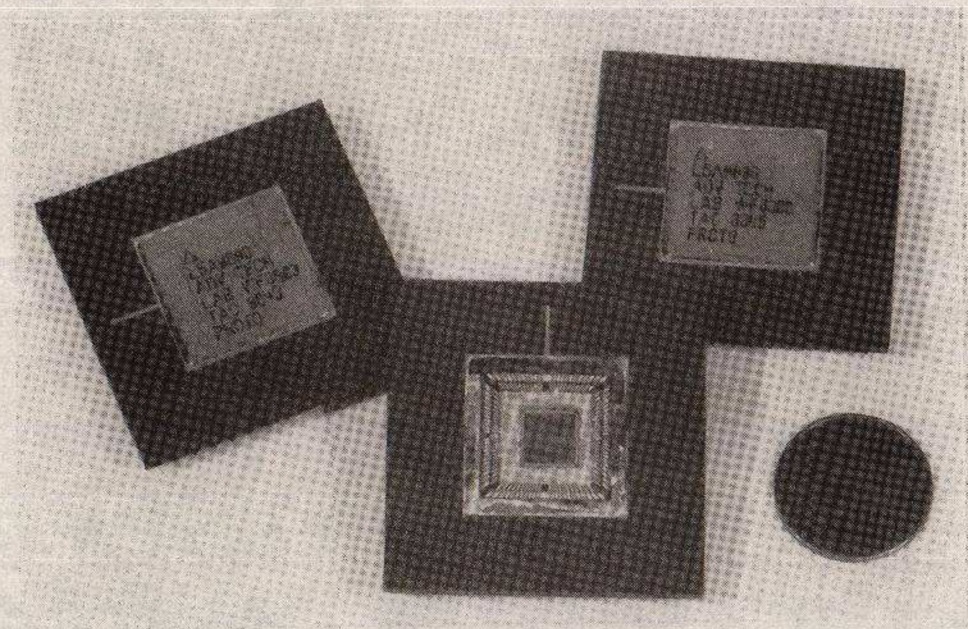


Figure 11 - WAVE ASIC Photograph

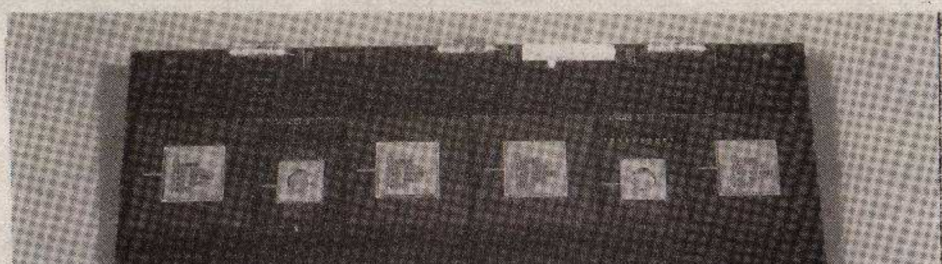


Figure 12 - WAVE ASIC Processing Card

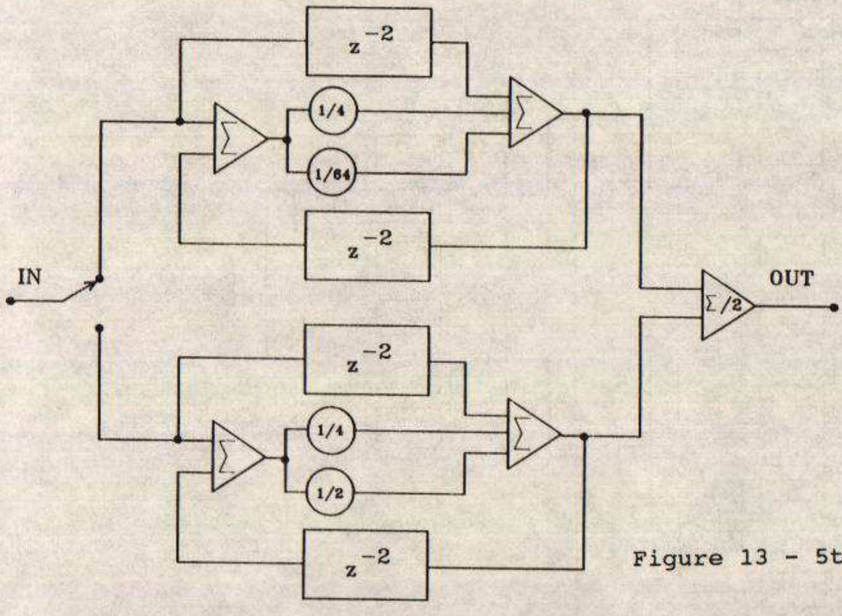
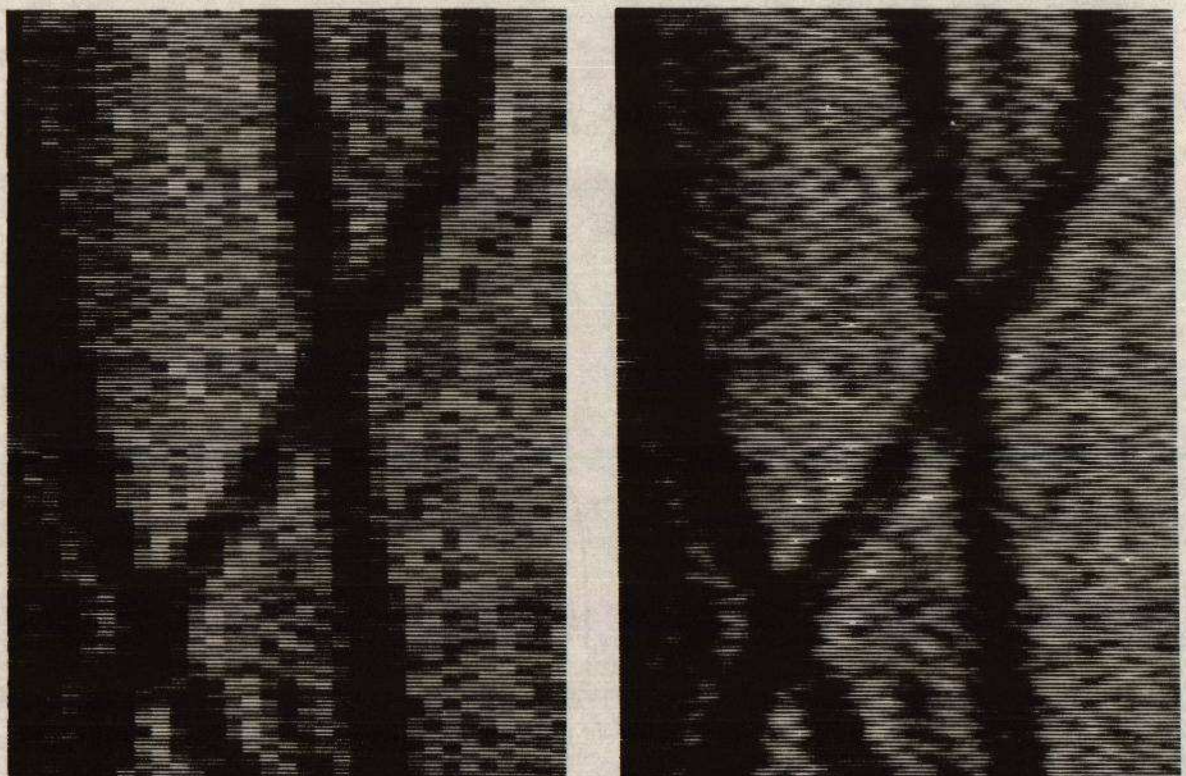


Figure 13 - 5th Order Canonic Signed Digit Schematic



Raw P-Theta Display

Interpolated P-Theta Display

Figure 14

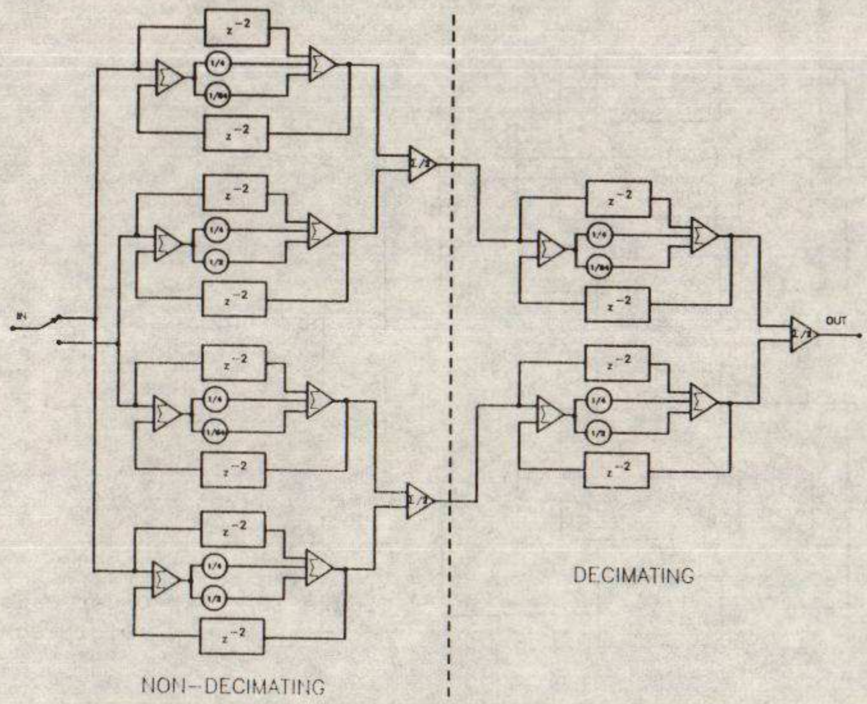


Figure 15(a) - High Performance CSD Implementation - Schematic

Figure 15(b) - High Performance CSD Implementation - Response