Proceedings of The Institute of Acoustics

HIGH POWER TRANSMITTERS FOR SECTOR SCANNING SONAR SYSTEMS

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1. Introduction

The motivation for the work reported in this paper first became apparent in the early 1970's. At this time, it became clear that it would be necessary to provide a replacement for an original transmitter equipment associated with the 300 KHz sector scanning sonar system on loan from the Admiralty Research Laboratories to the Ministry of Agriculture, Fisheries and Food and installed on R.V. Clione. The specification of the ARL equipment which employed vacuum tube technology was for output pulses of 20kW rms power level with pulse repetition time not shorter than 0.25 seconds, of duration 50 to 200μs with a nominal output of 100μs. A replacement system, again using vacuum tube technology had been built by MAFF but this did not wholly satisfy the design requirements. A transmitter using solid-state techniques seemed to offer a number of advantages in that both size and overall power consumption would be lower. An additional benefit was the potential of having a design which could be operated over a wide range of frequencies and power levels. All of these design aims have been satisfactorily achieved.

2. Consideration of Potential Output Stage Operation

In this section we consider the possible modes of operation of the power output stage. Of the linear modes, the high power dissipation of class A systems and the unnecessary complexity of class AB stages in order to have unwanted low distortion made it unlikely that either of these design techniques could be fruitfully employed. The known benefits in class B or C operation of low standby power requirements coupled with wide availability of skeleton circuits albeit for use at lower frequencies made these techniques attractive. These circuits can, however, only operate satisfactorily with low drive impedance on the bases of the output transistors in order to counteract the Miller effect resulting from the base-collector capacitance. This effect becomes increasingly important at higher frequencies. Solutions could involve the use of common-base rather than common-emitter configurations but this only emphasises the need for low drive impedances. One method of obtaining the necessary low impedance is through the use of the impedance-transformation properties of transformers for either the CB or CE arrangements. The desire for a wide range of operating frequencies and the unknown leakage parameters of the transformers made this design technique finally unattractive though it is, no doubt, possible to engineer satisfactory output stages using these concepts.

Last of all, we consider the use of class D in which the power output stage consists of transistors operated in the switching mode. For this design, it proved most convenient to use the current switching mode, the transistors switching between zero current and some acceptable upper limit of I amps.

Low impedance base drive for the output transistors was fairly easy to arrange using high current switching transistors operating between collector saturation voltages and cut-off - i.e. voltage switching mode.

The arrangement of the output transistors in the output stage is also an important consideration at the design stage. Three were considered as shown in figure 1;

(i) Two-transistor, two-capacitor bridge with transistors operated in the quasi-complementary mode,

(ii) Full-wave bridge operation using four transistors,

(iii) Push - pull operation using two transistors.

The necessity of using a transformer to couple to a piezo-electric transducer load allows any of these three arrangements to be used although (i) and (ii) are frequently used without a transformer. More complicated drive circuits are needed with (i) and (ii) because some of the transistors need base-emitter drive with a large common mode alternating voltage - e.g. the upper transistors in figure 1(ii). After several attempts, the most robust configuration was found to be that of figure 1 (ii).

3. Drive waveforms and Power output capability.

It is not desirable to operate the circuits of figure 1 with unity mark-space square waves since this would not allow any time for one transistor to switch-off before another started conduction. A period when both transistors of figure 1 (iii) are not conducting is therefore necessary for reliable operation. In addition, if the non-conducting interval has the duration of half of a conduction period, giving the drive waveforms of figure 2, it is possible in principle to reduce the third harmonic component of the load current waveform to zero although the higher harmonics are increased. The output power, p_{out} at the fundamental frequency may be calculated assuming a sinusoidal voltage of peak amplitude V_s on the collectors of T_1 and T_2 of figure 1 (iii) as a function of the non conducting portion of the cycle, u:

$$\begin{aligned} P_{out} &= \frac{1}{T}\int_0^T i(t)\ v(t)\ dt \\ &= \frac{2}{\pi}\int_0^{\frac{\pi}{2}} I\ V_s \sin\theta\ d\theta \\ &= \left[\frac{4}{\pi}\cos\left\{\frac{\pi u}{2}\right\}\right]\ \frac{IV_s}{2} \end{aligned} \qquad 3.1$$

The term in the square brackets of equation 3.1 represents the ratio of output power from the arrangement above to that from sinusoidal current and voltage waveforms having peak values I and V_s respectively. For u = 1/3 used in the present design, this factor is 1.103 and for a square wave drive (u=0), it is 1.273.

Current at the 5th and subsequent harmonics of the transmission frequency also flows in the load - a piezo-electric transducer resonant at the transmission frequency. The efficiency of the transducer at these harmonics is likely to be low and the resulting acoustic energy will suffer greater absorption than the fundamental component. We may therefore conclude that there is unlikely to be an acoustic problem. There is an electrical difficulty, however, in that the impedance of a normal piezo-electric transducer is high at electrical harmonics of its resonance. The load voltage waveform thus has a disproportionately high harmonic content. Since the voltage swing at the collectors of T1 and T2 is limited by the supply voltage and transistor ratings the high harmonic content will generally have the effect of reducing the fundamental component of the output voltage waveform. The load must therefore be arranged to have low impedance at the higher harmonics of the transmission frequency.

The duration of the interval during which both transistors should be non-conducting is approximately 0.5μs at 300 kHz. Transistors having switching times of this order at high power levels (typically several kVA) frequently have storage times, as opposed to rise and fall times, of many microseconds. Antisaturation measures must almost always be taken to prevent this switching penalty. The final circuit devised is shown in figure 3.

4. Output Stage Description

This section contains a description of a typical output stage as shown in figure 3. Transistors T_1 and T_2 are driven sequentially from a modulator of digital design through a low impedance drive circuitry. The collector currents of T_1 and T_2 are limited by R_1 and R_2. Collector current from the transistors is combined in the load through transformer TR1. The arrangement of diodes D_1, D_2 and capacitor C_1 is a passive anti-saturation circuit. If load conditions are such that the collector voltage tries to drop below $V_{as} - V_D$ either D_1 or D_2 conducts drawing the unwanted excess of collector current from C_1 which has a large capacitance. The state of charge of C_1 is maintained by the power supply which recharges it during the inter-pulse interval. The main energy for transmission is drawn from C_2 which is also recharged during the interval between pulses. The diodes D_3 and D_4 and the zener diode D_5 (with a voltage rating similar to V_{cc}) are intended to prevent over voltage conditions of the collectors of T_1 and T_2 due to the leakage reactance of TR1. The capacitor, C_3, also helps to limit switching surges on the collectors of T_1 and T_2 and furthermore helps to provide a low impedance at the higher harmonics of the transmission frequency. It is anticipated that a change in frequency would require both TR1 and C_3 to be changed.

This circuit can be arranged to operate satisfactorily with an open-circuit load condition by ensuring that sufficient energy is stored in C_1 to prevent the power transistors entering the saturated region of their characteristics during a transmission. Operation with a short-circuited load condition may be guaranteed in one of two ways. The simplest is choose transistors which have a safe operating area (SOAR) which allows an interval longer than the pulse duration at I and V_{cc}. This region is normally the one controlled by the secondary breakdown characteristics of the transistor.

In the event that the safe interval is too short for the pulse length desired, circuits can be arranged to detect the attempted transmission via the presence of voltage across R_1 and R_2, to detect the inadequate output voltage via a tertiary winding on TR1 and remove the drive from T1 and T2 within the safe interval at I and V_{cc}. Both these techniques have been successfully used.

The transistors which were finally chosen have the following characteristics:

BV_{cE} : 500V	Safe interval at 200V and 10A	: 300μs
I_{cmax}: 20A	t_{on} t_{off} $\frac{\Omega}{x}$ 0.3μs	
f_T : 20 MHz	h_{fe} I_c @ 5 amp = 10 minimum.	

The transistors were operated at 10A peak and with a supply voltage of 220V allowing a reasonable safety margin. The allowed collector voltage swing was 200V giving an output power per pair of transistors of 1.1 kW. In order to achieve the necessary 20kW of output, it is thus necessary to use twenty pairs of transistors (making 40 transistors in all). The best compromise in terms of minimising the cost and complexity of the drive circuitry involves the use of a pair of transistors in the T_1 location and another pair in the T_2 position. Separate emitter resistors were used to ensure satisfactory current sharing. This output circuit together with the drive circuitry and power regulating systems for charging C_1 and C_2 comprised a 2kW module. The complete transmitter uses 10 such modules each driven from the same power supply and modulator. The outputs from each module were combined simply by parallel connections to each output transformer so that the current output from the power transistors added in phase.

This parallel path system can be made robust against a failure in one or more 2kW modules by disconnecting the offending modules from the output bus using a relay. Failure in a module was sensed through the voltages of the various supplies internal to the module. This was generally proved to be a satisfactory arrangement, with the exception of those infrequent failures which demand a heavy load from the power supply.

5. Drive Circuits and Modulator

The modulator whose role is illustrated in figure 4 produces all the necessary signals to operate the power output stage at TTL levels. Three signals only are needed, of which two are of the type illustrated in figure 2 having the duration of the pulse length required. The third signal is an enabling one which switches the drive circuits into an active mode a few ten of microseconds before the pulse is transmitted and returns them to a quiescent condition several hundred microseconds after the transmission. This arrangement has the advantage of holding down the average power requirements of the drive circuitry which would otherwise have been considerable and yet allows sufficient time (greater than 6 time constants) for the cooling of the power output transistor junctions.

The modulator system has evolved most of all during the development of the system starting as a relatively modest affair using a crystal clock to define the transmission frequency and monostable multivibrators to define the pulse duration and repetition intervals. The final version has a sequence of pulse duration and repetition intervals programmed on Read-only memories. It is capable of being remotely operated with the status of the controls being read just before a transmission and has a status output port for use by a computer. The next stage, which we have not yet undertaken, would be to provide full computer control as well as the manual control option.

The drive circuitry has also evolved during the course of the work. The first systems used a mainly discrete component drive system employing magnetic memory drive transistors to switch the power transistors on and off. Integrated digital circuits with outputs of 24V and 0.75 amps have replaced the discrete memory drive transistor in many applications and the driver circuit has been altered to take advantage of this development. Early experience showed that a failure in a power output transistor would ripple-back several stages into the drive circuit and the opportunity of redesign has allowed us to avoid this undesirable fault behaviour. The integration of the drive circuitry has improved the reliability by a significant factor.

6. Conclusions

About 10 of these transmitter systems are now operational having the following range of characteristics (not all simultaneously available!)

Power output	2, 4, 20 kW
Transmission frequency	30 to 300 kHz
Pulse duration	50μs to 3ms
Pulse repetition interval	150ms to 2 secs
Power supply	24V dc (nominal) or 220 volts (nominal) ac 50-60 Hz.

The circuits appear to be generally reliable with those having the integrated circuit drivers certainly better than the earlier discrete device drivers. Quite a few problems have been caused by the plugs and sockets used for the interconnection of the power output modules and the rest of the system. In retrospect it might have been advantageous to design the power output modules to withstand insertion into or withdrawal from the system while it is operating. Perhaps this can be done on the next range of systems.

FIG.1(i)

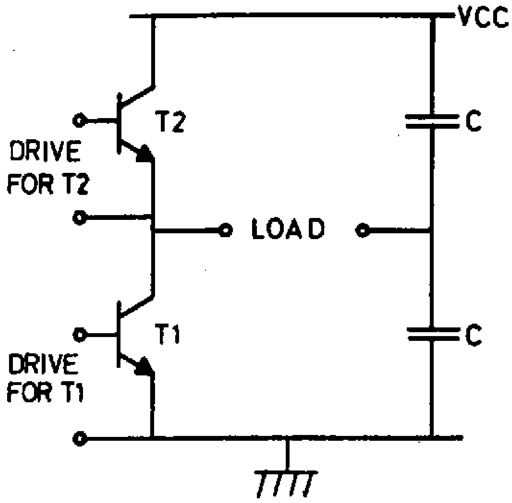


FIG.1(ii)

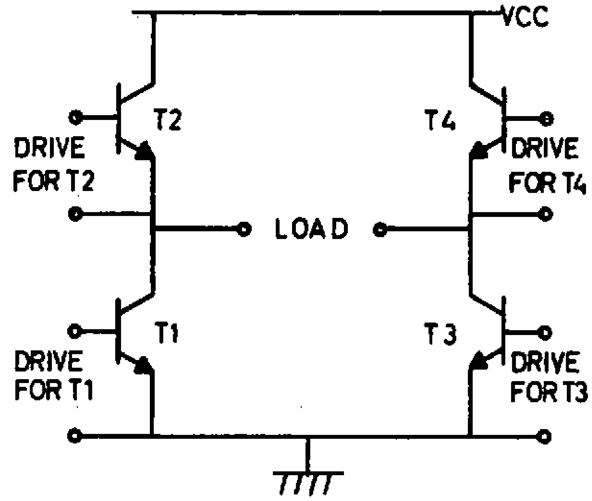


FIG.1(iii)

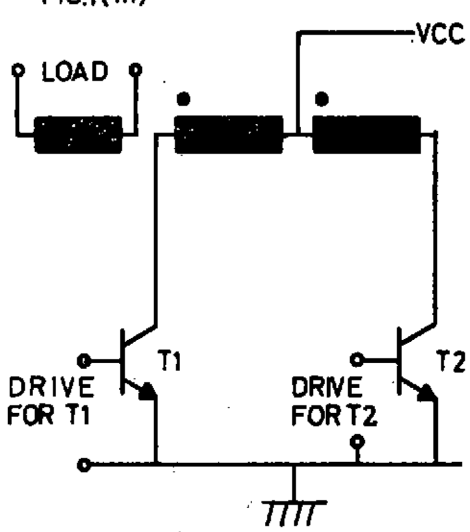


FIG.2

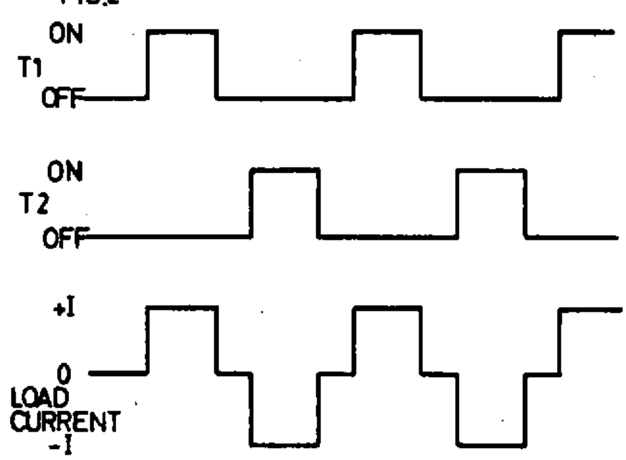


FIG.3

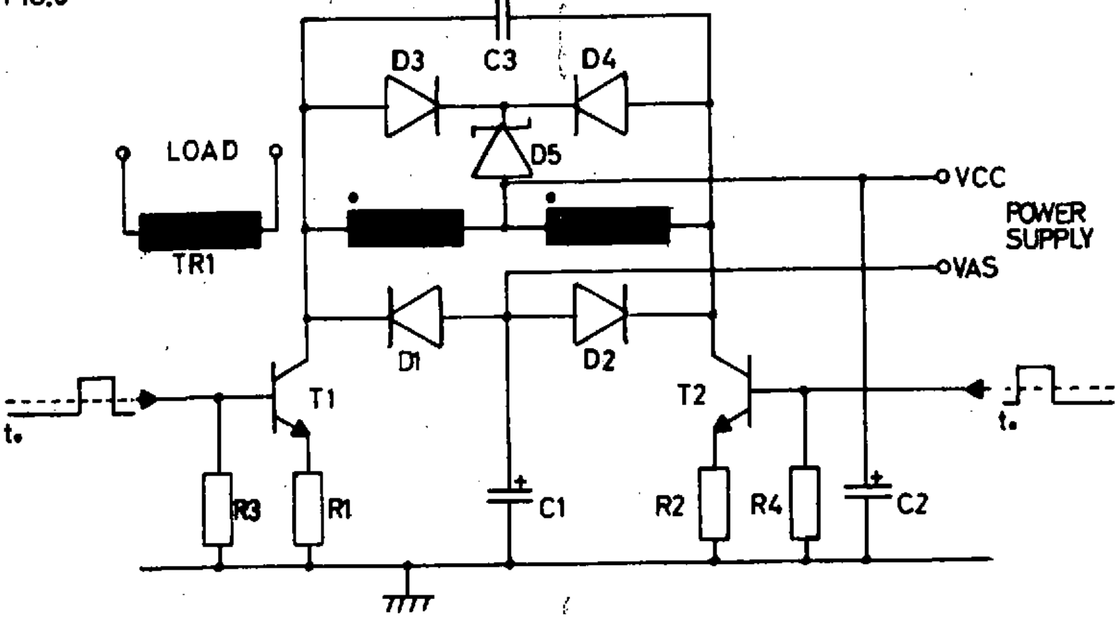
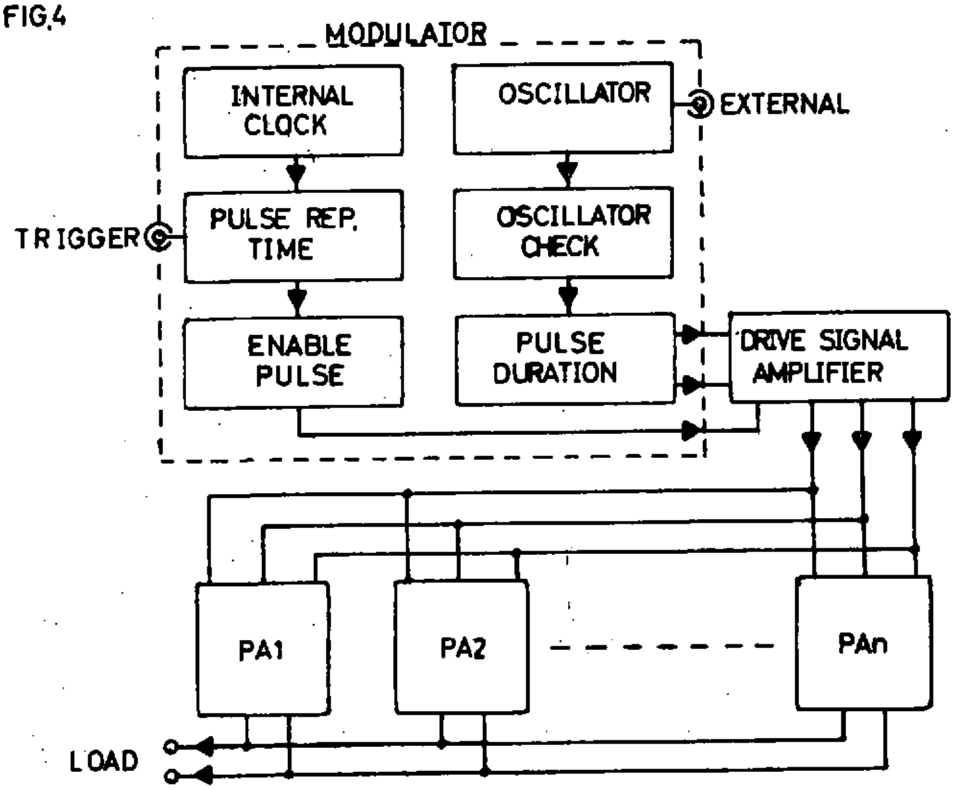

C3
D3
D4
D5
LOAD
TR1
VCC
POWER SUPPLY
VAS
D1
D2
T1
T2
t₀
R3
R1
C1
R2
R4
C2

FIG.4


MODULATOR
INTERNAL CLOCK
OSCILLATOR
EXTERNAL
TRIGGER
PULSE REP. TIME
OSCILLATOR CHECK
ENABLE PULSE
PULSE DURATION
DRIVE SIGNAL AMPLIFIER
PA1
PA2
PAn
LOAD