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INTERFACE REQUIREMENTS FOR A TRANSIENT RECORDER

D. J. OLDHAM

DEPARTMENT OF BUILDING SCIENCE, UNIVERSITY OF SHEFFIELD

INTRODUCTION

In recent years the microcomputer has become established as an essential item in the well equipped acoustic laboratory. In general they have been purchased initially to aid routine calculations but more often than not they find themselves being applied to the running of experiments. It is now quite common to find an inexpensive microcomputer controlling an experiment involving signal generators and frequency analyzers costing considerably more.

In addition to employing microcomputers to control other equipment via standard interfaces, such as the IEEE 488 Bus, a number of experimenters have discovered that it is comparitively easy, given modern integrated circuits, to construct devices which extend the capabilities of their existing, and possibly dated, equipment. This paper describes such a device, a programmable digital transient recorder for use with the Commodore PET computer.

THE TRANSIENT RECORDER

A digital transient recorder consists essentially of an analogue to digital converter and a block of read/write memory. The analogue signal to be recorded is sampled at regular intervals by the analogue to digital converter and the resultant digital word is stored sequentially in the memory. At the end of the sampling process there is thus a digital representation of the signal stored in the memory which can be accessed and displayed on an oscilloscope or transferred to a computer for processing.

It is possible to employ a microcomputer and analogue to digital converter as a transient recorder with the analogue to digital converter placing its signal directly onto the computer's data bus from which it can be transferred into the computer's memory. Objections to this approach are largely concerned with speed. Operation in BASIC is not feasible and a machine language subroutine must therefore be employed. The sampling rate may still not be adequate, particularly if an analogue to digital converter of more than eight bits resolution is employed or if it is desired to simultaneously record more than one channel of information.

The device described in this paper circumvents this problem by employing an external block of RAM for data storage. The RAM can store the information in whatever word length is desired and can be arranged to store any number of simultaneously recorded signals.

The key to the device lies in the use of the microcomputer's clock to control the sampling rate. The user port of the PET is part of a 6522 versatile interface adaptor. This chip features an internal parallel input-serial output shift register. Data is loaded into the shift register and it is then shifted out onto the CB2 line under the control of an internal timer. The shift register acts in cyclical manner with the output from bit eight being fed back to bit one. The rate at which data is shifted out onto the CB2 line is determined by the contents of the timer. The timer is a presetable counter which counts the number of clock pulses. On each clock pulse the counter is decremented, when the contents of the counter is zero a pulse is output to the shift register thereby shifting the contents one bit to the right. At the same time the timer is reset to its initial value and then the process is repeated.

In this way a repeated pattern of eight bits can be shifted out into the CB2 line at a particular frequency and totally independant of processor control. By loading the shift register with 00001111 and the timer with 255 a square wave of frequency 490 Hz can be generated. The highest frequency is obtained by setting the shift register to 01010101 and the timer to 1 giving a square wave output of 500 kHz.

Figure 1 shows a schematic of the system. Pulses from the CB2 line are used to initiate the analogue to digital conversion process. The same pulses are also used to drive a binary counter the output of which is used to address the memory block. Lines from the PET's IEEE 488 port are used to set the required binary count and to write enable the RAM. The extension of the system to two or more channels requires the provision of additional RAM and analogue to digital converters, the former addressed by the same binary counter and the latter driven by the CB2 pulses hence assuring perfect synchronisation.

TRANSFER OF DATA

Data can be transferred from the external RAM to the computer via the eight data lines of the user port either relatively slowly under BASIC or by means of a machine code subroutine. Alternatively the data lines of the external RAM can be used to drive a digital to analogue converter so that the signal can be examined on an oscilloscope or recorded by means of a chart recorder. The easiest way to address the RAM is again using the binary counter but to ensure a sufficiently slow rate to enable the data to be taken up by the computer the CB2 line has to be driven by another technique. This can be done in BASIC, for example by the commands POKE 59468, PEEK (59468) AND 31 or 224 (which sets CB2 high) or POKE 59468, PEEK (59468) AND 31 or 192 (which sets CB2 low).

CONCLUSION

The device described in this paper enables low cost efficient recording of transient data. In use it would act as an interface between standard analogue acoustic instrumentation and a microcomputer.

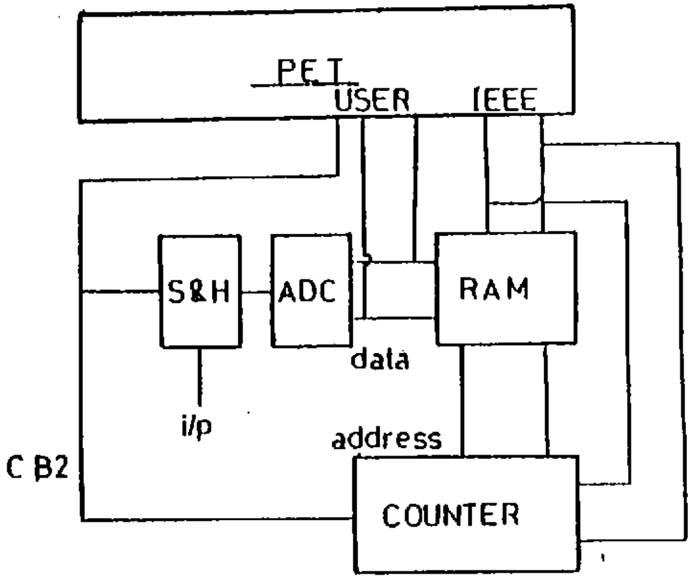

FIG 1