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AN ULTRASONIC WIRELESS DATA FEEDTHROUGH SYSTEM BASED ON FIELD PROGRAMMABLE GATE ARRAY

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This paper proposes an ultrasonic wireless data feedthrough system based on field programmable gate array (FPGA). This system can transmit information through metal barriers without physical penetrations by using ultrasound. Lead zirconate titanate (PZT) transducers are used to complete the conversion between electricity and ultrasound. And the system achieves a high data rate by using FPGA. Besides, single-carrier frequency domain equalization (SC-FDE) technique is used by the proposed system. And because of this, the transmitter of the proposed system is less complex and lower power than that of an orthogonal frequency division multiplexing (OFDM) system. Therefore, the proposed system could work for a long time even under battery-powered conditions. A prototype system is built, and it is capable of transmitting data at 256 kbps through a 40-mm thick steel barrier. The proposed system could be used in a wide range of commercial, industrial, and nuclear applications to preserve structural integrity and improve safety.
Keywords: wireless data feedthrough, ultrasound, PZT transducers, SC-FDE, FPGA

1. Introduction

The traditional wireless technologies use radio frequency (RF) signal which is ineffective for communicating through a solid metal barrier due to the shielding effect of the metal. Ultrasound is a kind of mechanical wave which can propagate in metal. And recent researches have proved that ultrasound is capable of transmitting data through metallic barriers [1]. But the multipath propagation in the acoustic-electric channel caused by reflection limits the communication rate [2]. To increase the transmitting date rate, orthogonal frequency division multiplexing (OFDM) technique was used in [3] and [4], and data rates of 15 Mbps and 17.37 Mbps are achieved, separately.

Although OFDM has a higher spectral efficiency, it is less robust than SC-FDE against impairments from non-linear power amplifiers, IQ imbalance and ADC resolution [5]. Especially, the power requirement of SC-FDE technique in transmitter is much less than OFDM technique [6, 7]. In this paper, we propose an ultrasonic wireless data feedthrough system based on SC-FDE technique, which is suitable in an environment without sufficient power supply, such as outside the body of a ship or inside a pressure vessel. To achieve a high data rate, the proposed system is implemented on FPGA.

The implementation of the proposed system is detailed in this paper. Section 2 describes the structure of the system. And Section 3 provides details of the important parts of the system. Then, a prototype system is demonstrated in Section 4. Finally, a conclusion is drawn in Section 5.

2. System structure

The structure of the proposed system is presented in Fig. 1. At the top of Fig. 1 is the transmitter; at the bottom is the receiver; and in the middle is the acoustic-electric channel. The channel consists of a transmitting ultrasonic transducer, a metal barrier and a receiving ultrasonic transducer. And this channel structure is commonly called a sandwiched plate piezoelectric transformer (SPPT) [8].

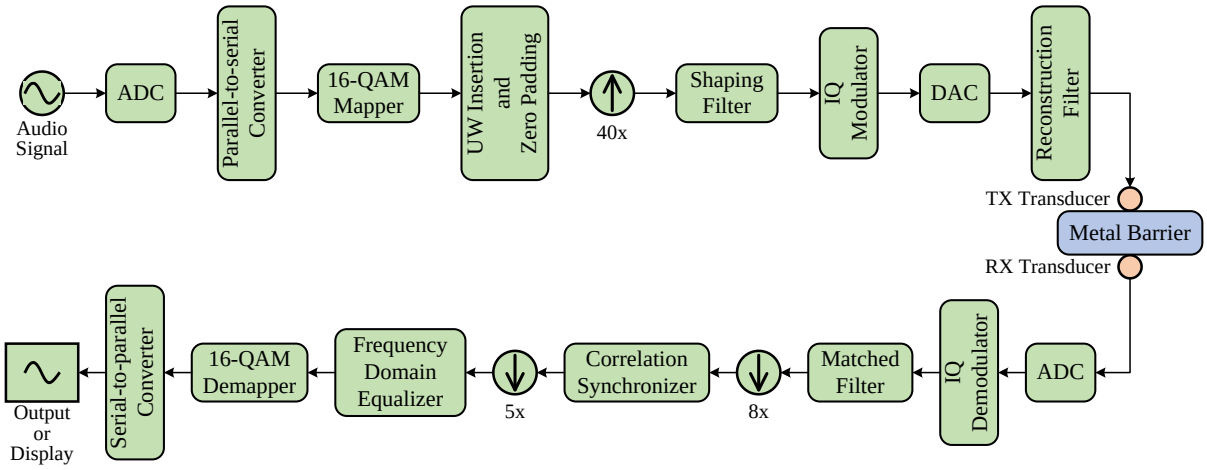

Figure 1: System structure.

The proposed system is designed to transmit audio signal (such as voice or noise signal) through a metal barrier, so an audio analog-to-digital converter (ADC) is used as the input module of the transmitter. The sampling rate and the resolution of the input ADC are 16 kHz and 16 bits, respectively. And the system uses 16-QAM to improve the spectral efficiency. Because each symbol in the 16-QAM alphabet carries 4 bits of information [9, 10], the ADC samples are first parallel-to-serial converted, and then 16-QAM mapped. Next, the QAM symbols are framed by periodically inserting unique word (UW) sequences and padding zeros, for synchronization and equalizer training purposes [11]. The framed signal is then up-sampled by a factor of 40 and shaped by a square-root raised cosine (SRRC) filter. Afterwards, the shaped baseband signal is modulated to the carrier frequency by the IQ modulator. The modulated signal is then passed through a digital-to-analog converter (DAC) and a low-pass reconstruction filter, which convert the digital signal into a synthesised, analog signal to drive the transmitting transducer.

The transmitting transducer converts electrical energy into mechanical energy, in the form of ultrasound, which easily propagates through the barrier and is subsequently converted back into electrical energy by the receiving transducer [12].

The output of the receiving transducer is first pre-amplified and then digitized by an ADC at the same sampling rate as the transmitting DAC. Next, the digital signal is down-converted to baseband by the IQ demodulator followed by the matched filter. The matched filter and the shaping filter are implemented to overcome the effect of inter-symbol interference (ISI), and they are identical SRRC filter [13, 14]. The baseband signal is then down-sampled. And the frame timing is synchronized by taking correlation between the down-sampled baseband signal and local UW sequences [15]. The synchronized signal is then down-sampled and equalized in frequency domain, compensating for channel fading and distortion [16]. Finally, the equalized signal is recovered to binary data stream by the 16-QAM demapper followed by a serial-to-parallel converter. The recovered data could be transmitted to a later system (such as a DSP system) or output to a host computer for display and storage.

3. System implementation

The implementation detail of the proposed system will be described in this section. In the transmitter, five modules will be described: the parallel-to-serial converter, the 16-QAM mapper, the UW inserting and zero padding module, the shaping filter and the IQ modulator. In the receiver, the correlation synchronizer and the frequency domain equalizer will be elaborated. The other modules are similar to corresponding modules in the transmitter and not described for simplicity.

3.1 Transmitter

3.1.1 Parallel-to-serial converter

The timing of the parallel-to-serial converter is shown in Fig. 2. The signal "clk_16k" is the output clock of the input ADC, the signal "clk_64k" is the output clock of the module, the bus "parallel_in" is the 16-bit wide input bus and the bus "serial_out" is the four-bit wide output bus. The bus values are represented in hexadecimal notation. The frequency of the signal "clk_64k" is 64 kHz, which is four times that of the signal "clk_16k". Besides, the phase relationship between the two clocks is marked in Fig. 2. At each rising edge of the signal "clk_64k", the module outputs four bits of the data on the bus "parallel_in"; and in each period of the signal "clk_16k", the data on the bus "parallel_in" is output from the high-order four bits to the low-order four bits.

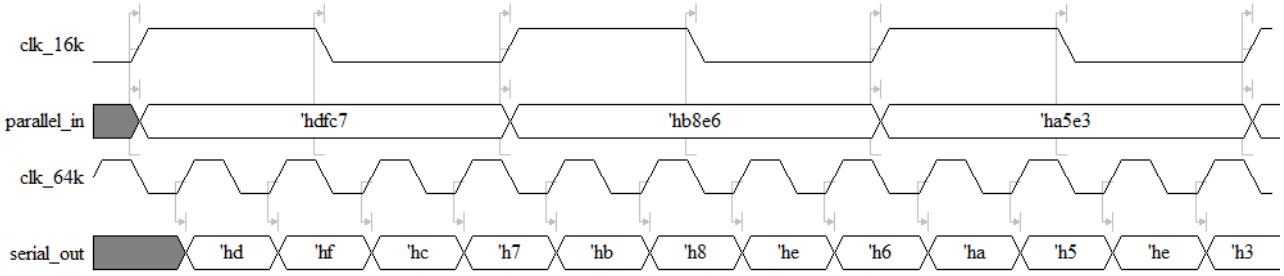

Figure 2: Timing of the serial-to-parallel converter.

3.1.2 16-QAM mapper

The QAM constellation used in the proposed system is shown in Fig. 3. The high-order two bits of the binary data correspond to the in-phase component, i.e. the abscissa; while the low-order two bits correspond to the quadrature component, i.e. the ordinate. Because the output bit-width of the module is set to 13 bits, the coordinates are selected from the set {-3072, -1024, 1024, 3072} in order that the Euclidean distance between each two constellation points is as large as possible.

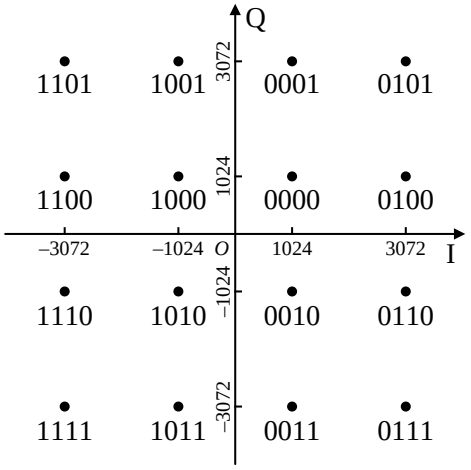

Figure 3: 16-QAM constellation used in the proposed system.

3.1.3 UW inserting and zero padding module

Figure 4 shows the frame structure of the proposed system. Each frame carries 1024-symbol modulated user data, so the frame rate is

$$\frac{64\ \text{ksymbol/s}}{1024\ \text{symbol/f}} = 62.5\ \text{f/s}\,. \tag{1}$$

And because the data rate after UW insertion and zero padding is set to 125 ksymbol/s, the frame length equals

$$\frac{125\ \text{ksymbol/s}}{62.5\ \text{f/s}} = 2000\ \text{symbol/f}\ . \tag{2}$$

Furthermore, three 64-symbol UW sequences are inserted in each frame for synchronization and equalization purpose. Two of these sequences are inserted before the user data part; the left one is inserted after the user data part. These UW sequences are composed of Chu sequences [11]. The remaining symbols at the end of a frame is padded with zero values, and the length of these values is

$$2000\ \text{symbol} - 64\ \text{symbol} \times 3 - 1024\ \text{symbol} = 784\ \text{symbol}\,. \tag{3}$$

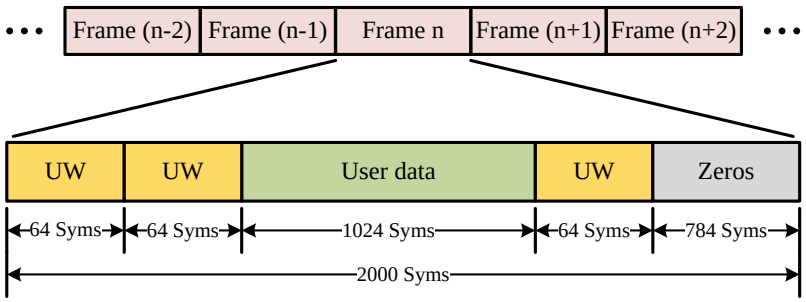

Figure 4: Frame structure.

3.1.4 Shaping filter

The impulse response of a SRRC filter is expressed as

$$h_{srrc}(t) = \frac{\sin\left[\frac{\pi t}{T}(1-\alpha)\right] + 4\alpha\frac{t}{T}\cos\left[\frac{\pi t}{T}(1+\alpha)\right]}{\frac{\pi t}{T}\left[1-\left(4\alpha\frac{t}{T}\right)^2\right]}, \tag{4}$$

where α is the roll-off factor and T is the symbol period [9, 17]. Taking into account the logic resource cost, the roll factor and the length of the filter used in this module are set to 0.5 and 161, respectively. In addition, a delay is inserted to make the filter physically realizable. Figure 5 shows the normalized impulse response of the filter. In the implementation, the system further reduces the number of multipliers from 161 to 81 by using the impulse-response symmetry.

3.1.5 IQ modulation

An IQ modulator modulates a two-dimension vector signal onto a scalar carrier signal [9]. The structure of the IQ modulator in the proposed system is shown in Fig. 6, where the carrier frequency *f* equals 500 kHz. Firstly, the two numerically controlled oscillators (NCOs) generate the in-phase carrier and the quadrature carrier, respectively, using the sample values stored in on-chip ROMs. Secondly, the module multiplies the two carriers separately with the in-phase input and the quadrature input. Finally, the module adds the two products together and gets the scalar output.

3.2 Receiver

3.2.1 Correlation synchronizer

The principle of this module is to determine frame start positions according to the peak values of the cross-correlation function of the received signal and the UW sequences. Figure 7 shows the structure of the correlation synchronizer.

IN_I and IN_Q represent the in-phase component and the quadrature component of the vector input, respectively. Two series of shift registers separately register the two components. These shift register series are the same; and each of them is a cascade of 127 shift registers with depths of five and a shift register with a depth of n. The module stores locally the conjugate values of two cascaded UW sequences, expressed as UW_0^*, UW_1^*, UW_2^*,…, UW_{127}^*. In each period of the input clock (not shown in Fig. 7), the data at all the junctions are complex multiplied by the corresponding conjugate UW values, generating 128 products. Then the adder sums all the products and obtains a value of the cross-correlation function.

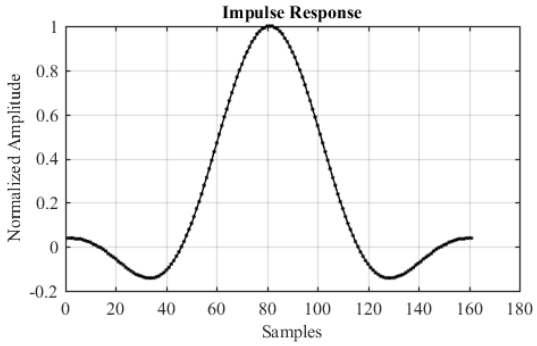

Figure 5: Impulse response of the SRRC filter.

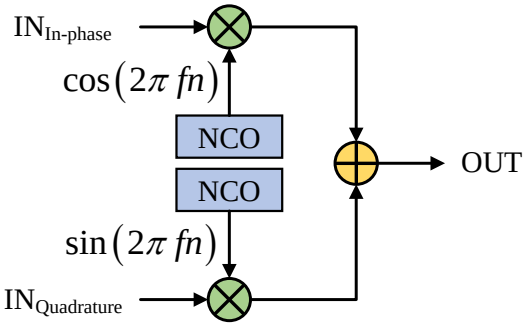

Figure 6: Structure of the IQ modulator.

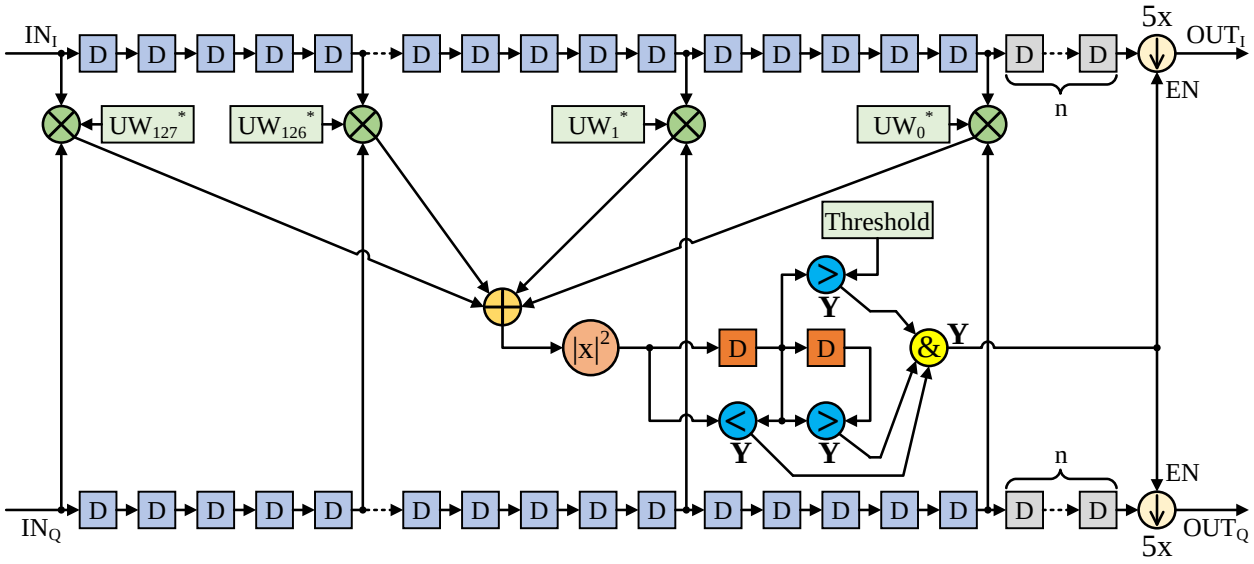

Figure 7: Structure of the correlation synchronizer.

After that, the square-of-modulus calculator, which is marked as $|x|^2$ in Fig. 7, converts the complex values into real values in order to compare their magnitudes. The squared values are sent into a shift register with a depth of two. At a certain moment, if the first value is the maximum among the values at the center tap, the input point, the output point of this shift register and the locally stored threshold, it is the peak value of the squared magnitude of the cross-correlation function in the current frame period.

The last two shift registers is used to ensure that the module starts to output a frame simultaneously with the catch of a peak value. So, the number n equals to the sum of the latencies of the complex multipliers and the sub-modules after them. In addition, the depths of the front 127 shift registers are

all five, because the synchronization module's input data rate is five times the baseband rate. And when outputting, the module down-samples the synchronized data to baseband by a factor of five.

3.2.2 Frequency domain equalization

The frequency domain equalizer is adopted to cope with channel fading in the proposed system. Figure 8 shows the diagram of the frequency domain equalizer.

The input signal is sent to three separate paths: one leads to a 64-point FFT sub-module, another leads to a 2048-point FFT sub-module and the other leads to a counter. The counter controls the whole operation of the module. It begins to count from zero once a frame comes and resets after an equalization operation is finished. When the counter increases into the interval [65, 128], the 64-point FFT starts to read in the second UW sequence at the beginning of the current frame. After the computation is completed, the module divides the results of the 64-point FFT by the locally stored FFT results of the original UW sequence to obtain the 64-point transfer function values.

The top path only consists of a 2048-point FFT sub-module. Once the counter increases into [129, 1216], this FFT sub-module begins to read in data and compute. Then, the equalized frequency domain data could be obtained by dividing the results of this FFT by the transfer function values. However, these two series of data have different lengths. So, the equalizer uses three additional sub-modules to extend the length of the transfer function from 64 to 2048. Furthermore, the sum latency of the bottom path is obviously longer than that of the top path. Therefore, the top FFT sub-module waits for the bottom 2048-point FFT to synchronously output results. Finally, a 2048-point IFFT transforms the results from frequency domain to time domain, obtaining the equalized data.

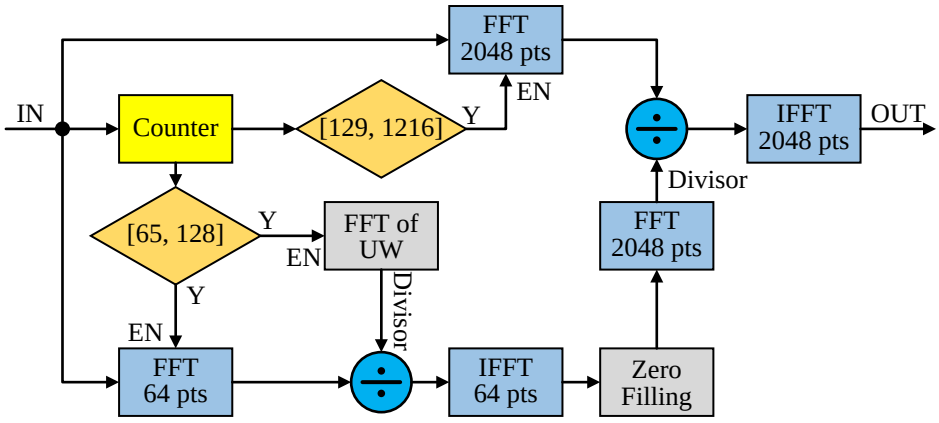

Figure 8: Diagram of the frequency domain equalizer.

4. System validation

A prototype system is built to validate the design of the proposed system. As shown in Fig. 9, the transmitter is implemented on a custom-designed board based on Altera Cyclone II family EP2C70F672C8 FPGA. The acoustic-electric channel consists of a 304 stainless steel plate and two Olympus A101S-RM piezoelectric transducers. The transducers are axial-symmetrically attached on the opposite surfaces of the plate. The size of the plate is 300 mm (L) ×300 mm (W) × 40 mm (T). The diameter and the center frequency of the piezoelectric element in A101S-RM are 1 inch and 500 kHz, respectively. The receiver is implemented using a Xilinx VC707 evaluation board and a TI AFE7225EVM evaluation board. The core device of VC707 is a Virtex-7 family XC7VX485T FPGA, and that of AFE7225EVM is an AFE7225 transceiver which consists of a two-channel ADC and a two-channel DAC.

The experiments are performed as follows. Firstly, the input port of the transmitter is connected to a function generator. Secondly, in the receiver, the demodulation output as well as the cross-correlation function value are wired to I/O ports of the FPGA and then connected to a logic analyzer. Thirdly, the function generator is set to continuous sine wave output mode; its output frequency and amplitude

are set to 1 kHz and 2 V_{pp}, respectively. Fourthly, the threshold stored in the receiver is adjusted according to the cross-correlation function values captured by the logic analyzer. Finally, the logic analyzer captures the demodulated sine wave, just as Fig. 10 shows. And the waveform captured by the logic analyzer changes correspondingly when the output frequency and amplitude of the function generator is adjusted. The communication rate is 500 kbps, and the effective rate is 256 kbps, excluding the UW sequences and zero blocks. In addition, the system obtains the designed target bit error ratio (BER) of 10^{-5}. It works normally without BER degradation after working uninterruptibly for eight hours. So it can be seen that the system can effectively and stably transmit data through a stainless steel plate without physical penetrations.

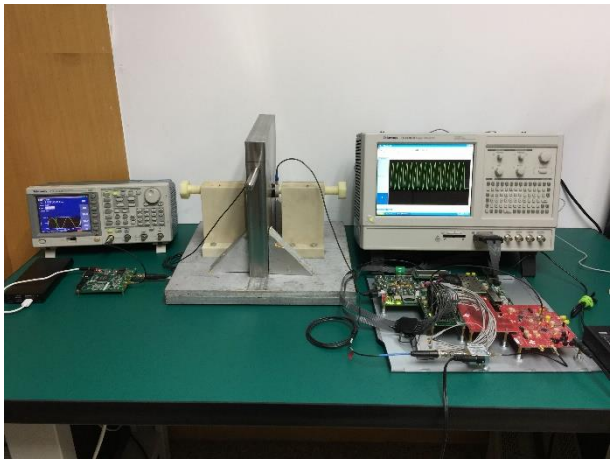

Figure 9: Hardware of the prototype system.

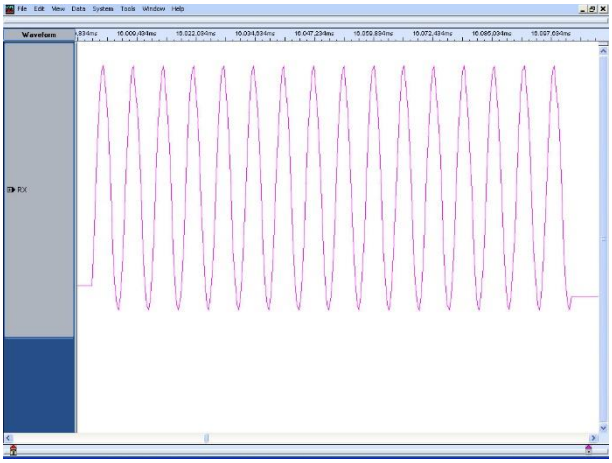

Figure 10: Waveform captured by logic analyzer.

5. Conclusion

In this paper, an ultrasonic wireless data penetration system based on FPGA is proposed, and a prototype system is built to validate the system design. The current communication bandwidth of the system is 500 kbps, which contains 256 kbps of user data.

The use of FPGA leaves lots of room for bandwidth promotion because FPGA has advantages of parallel processing. More importantly, the system uses SC-FDE technique, resulting in that the transmitter is lower complex and lower power than that of an OFDM system with the same performance. Therefore, the proposed system is more suitable for battery powered applications, such as transmitting data out from a sealed metal pressure vessel.

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