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EMC ON A PCB

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1 Introduction/Summary

This module will give the electronic engineer, technician or PCB draughtsman an appreciation of the EMC problems which can occur in the design of a single PCB and which will allow him/her to avoid them at the design stage; thus avoiding costly re-designs. The following topics are considered:

Coupling mechanisms and associated problems - Conducted (e.g. on supply), Capacitive and Inductive coupling, use of ground planes, local shields, supply decoupling, terminating signals;

Logic circuits - Logic families (TTL,NMOS,CMOS,& ECL) and their characteristics: problem sources and susceptibilities, fixes : terminating signals, noise-margins, circuit & track impedance, rise-time, & board layout;

Analogue circuits -Sources of EMI, susceptibilities, design to avoid problems: effect of circuit impedance, use of ground-planes, shields, guard tracks and improving board layout;

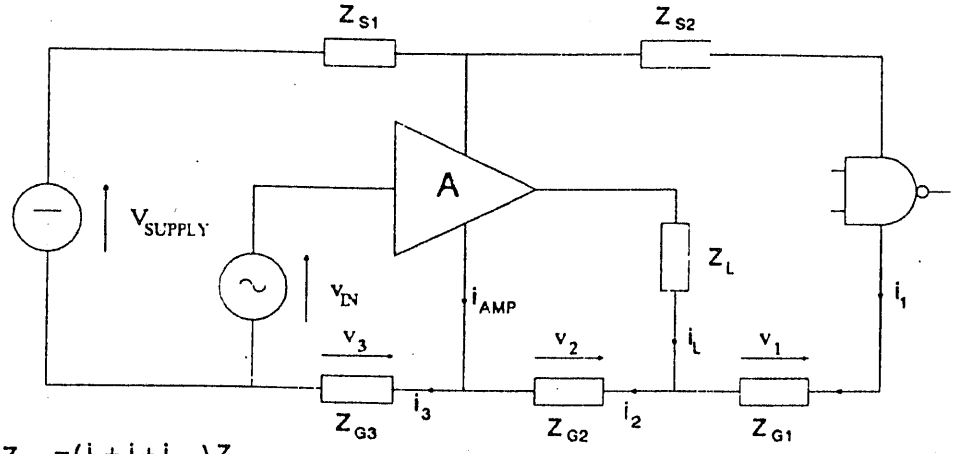
Although this section considers interference between components on a single PCB, the techniques described are also applicable to the reduction of radiated emissions from a PCB and its susceptibility to external sources EMI.

2 Coupling mechanisms

Here the various mechanisms by which interference can be propagated between sub-circuits on a circuit board are explained. The effect of board layout and ways of minimising coupling are considered. Specific problems encountered with analogue and digital circuits are addressed separately in sections 3 and 4.

2.1 Common impedance coupling

This usually occurs due to different circuits or components sharing the same ground or power supply lines. Fig. 1 shows the principle of common impedance coupling. The load current of a power amplifier is carried by the same PCB tracks as the power supply to the small signal stages; this results in variation of the supply voltage to the small signal stages at the signal frequency which may cause instability. Also noise due to switching of the logic gate is coupled back to the amplifier.



$v_3 = i_3 Z_{G3} = (i_1 + i_L + i_{AMP}) Z_{G3}$

Figure 1 Principle of common impedance coupling

Common impedance coupling can be minimised by three techniques:

a) reduction of common impedance values;
b) use of separate ground/supply tracks to susceptible circuits (star ground/supply connections);
c) use of separate supplies for susceptible circuits.

Figures 2a, 2b, 2c and 2d

Fig. 2a Small loops reduce supply inductance by reducing track length and by using mutual inductance to cancel line self inductance. Radiation and susceptibility is also reduced.

Fig. 2c Good power supply layout gives low supply impedance

Fig. 2b Large supply inductance due to long supply tracks and large loop area

Fig. 2d Poor and good PCB power supply layouts

Common impedance values can be reduced by increasing power supply track widths which reduces the track resistance and by using a power-track layout which minimises track inductance. Fig. 2 shows good and bad power supply track layouts. The inductance of the power supply tracks is reduced by keeping supply and return tracks close together so that their mutual-inductance cancels their self-inductances to some extent. Reducing the area of the loop formed by the power supply tracks also reduces pickup from external magnetic fields and radiation from the board itself. The use of power-supply planes in multi-layer PCBs provides the minimum supply impedance possible and greatly reduces common impedance coupling. When single or double sided boards are used power-supply planes, or even a single ground-plane, may not be possible. In such cases power supply line impedance can be reduced by the use of the separate low-impedance distribution buses which are available from a number of suppliers. These buses consist of two metal strips separated by a thin insulating layer with pcb-pins for mounting and power take-off. Both horizontal and vertical mounting types are available; the horizontal types are designed to run below IC packages mounted on a regular grid and so may be retro-fitted to many designs. As well as providing a low impedance supply the use of a separate distribution bus for power supplies mean that routing of other signals can be greatly simplified.

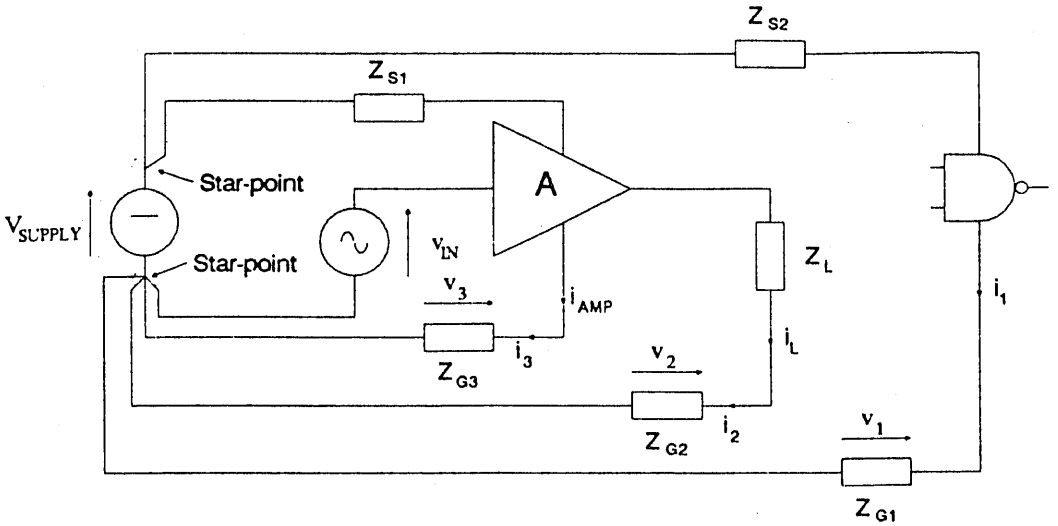
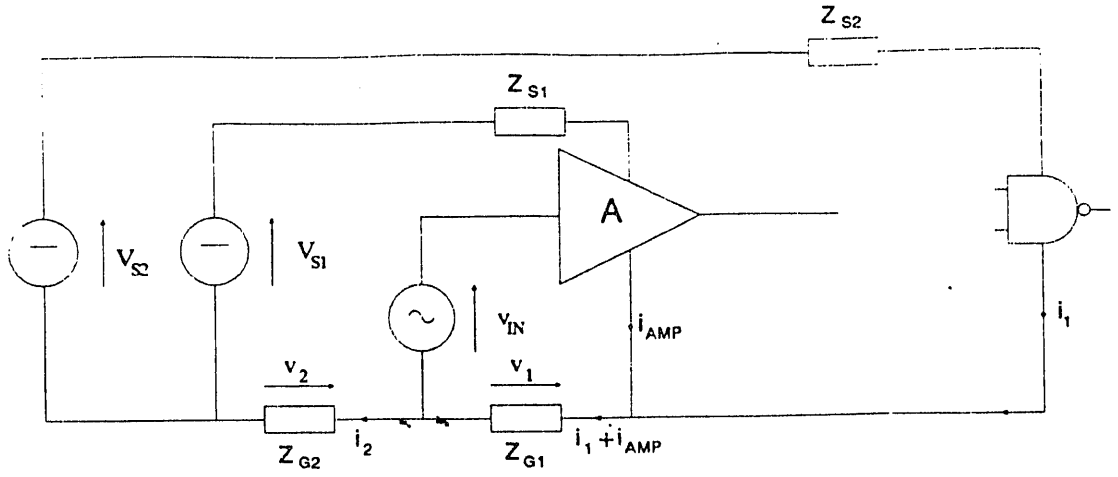


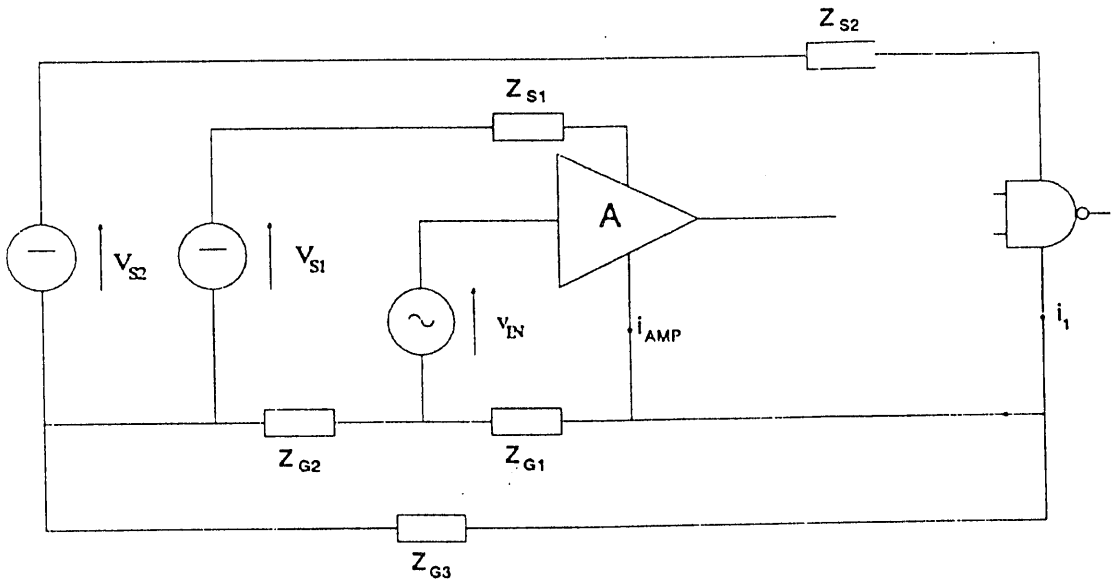
Figure 3 Reduction of common impedance coupling by using star ground/supply connections

The use of separate power and ground connections for susceptible circuits increases the complexity of the layout but may be necessary when power and small-signal circuits share the same power supplies. Logic circuits also draw large switching currents and are likely to require separate supply and ground tracks to prevent interference with small signal circuits. Fig. 3 shows the use of separate supply and ground tracks; in an ideal world the tracks would be separate all the way back to the power supply reservoir capacitor but if this is not possible a large decoupling capacitor at the star-point where the tracks meet can be used. Local decoupling capacitors near the susceptible circuit(s) may cause problems because they may act as a reservoir for the power circuit as well, causing unwanted currents to flow in the small-signal circuit supply/ground tracks. This can be alleviated by the use of a small resistor in series with the small-signal circuit supply track when local decoupling is required.

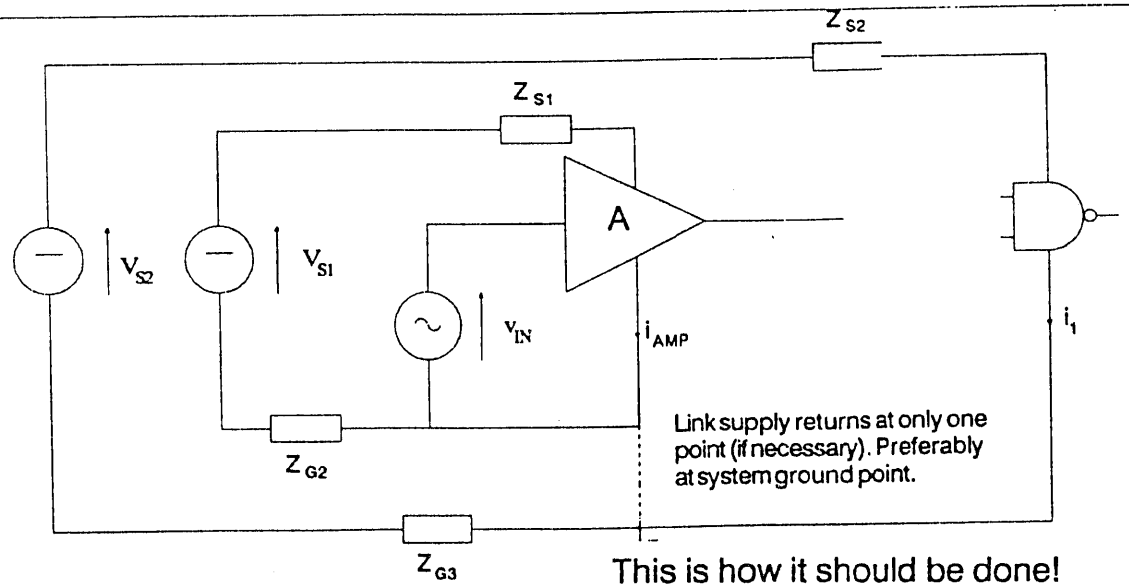
For particularly sensitive circuits which must operate on the same PCB as power or logic circuits (e.g. A-D converters and signal conditioning circuitry) then separate power supplies (Fig. 4) may be the only solution. The common or ground connections for each supply should be connected together at only one point (if a connection is required at all). If the supply common rails are connected at more than one point then the return current for the power circuit may flow in the small signal common track producing the common impedance coupling which we are striving to eliminate.



The wrong way to do it



Better but not quite right



This is how it should be done!

Figure 4 *Use of separate power to minimise coupling between circuits*

In considering common impedance effects it should be noted that the impedance of PCB tracks (or any other wiring system) increases with increasing frequency due to two factors:

a) the inductive reactance of the tracks increases with frequency;
b) skin effect increases the effective resistance of the pcb track at frequencies above about 10kHz.

Fig. 5 shows the effect of frequency upon track impedance.

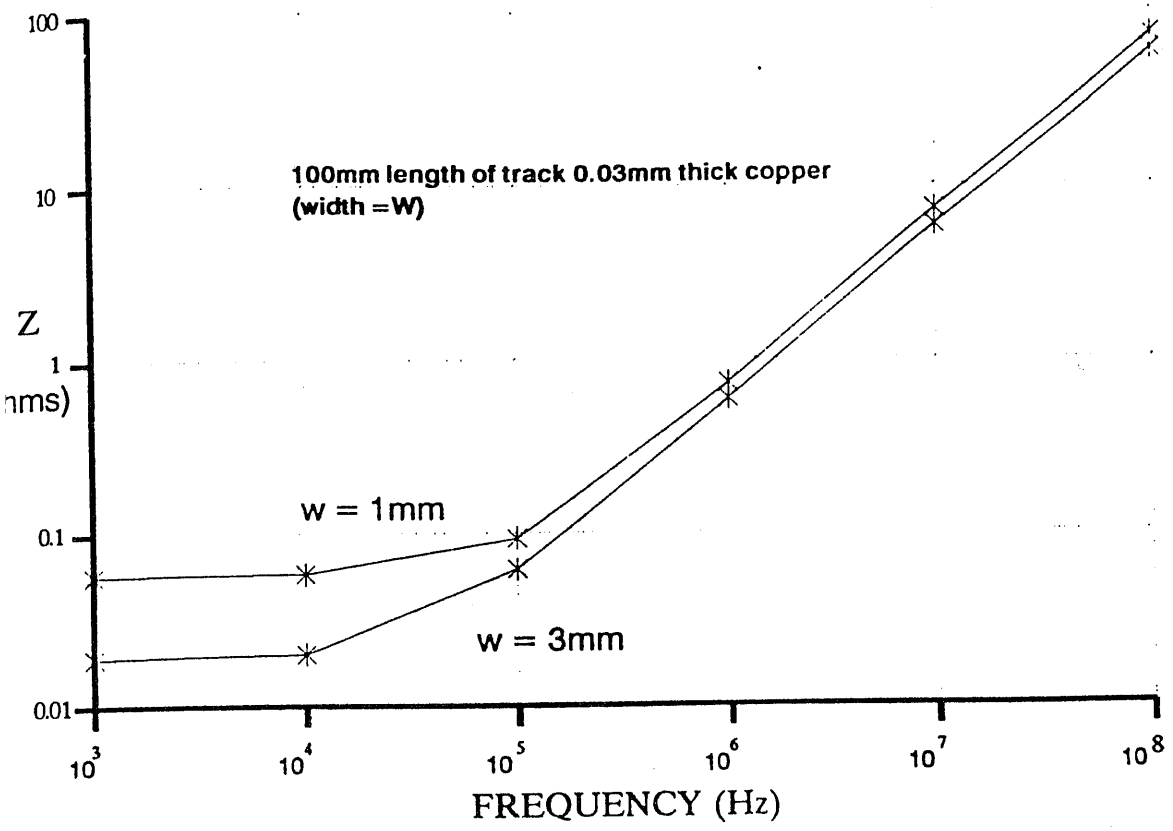


Figure 5 The effect of frequency upon PCB track impedance

2.2 Capacitive coupling

Any two conductors in proximity exhibit a capacitive coupling effect (Fig. 6). This applies not only to adjacent PCB tracks but also to components* and any other nearby conductors (e.g. heatsinks, mounting hardware, etc.). Any change in the potential of a source conductor causes a current to flow in the victim conductor which usually causes a change in potential at the victim. The current induced is given by the equation:

$$I_v = C_c \frac{dV_s}{dt} \qquad (1)$$

where C_c is the coupling capacitance, V_s is the source voltage and t is time. Capacitive coupling therefore increases with increasing rate of change of voltage in the source and so, circuits where dV/dt is great are the most likely sources (e.g. logic and switching circuits). Since dV/dt increases with frequency for a given sinusoidal signal, capacitive coupling effects are more likely in high frequency analogue circuits than in low frequency circuits. If dV/dt in potential sources can be kept as low as possible then the effect of the source can be minimised.

The change in potential of the victim circuit is dependant upon its impedance:

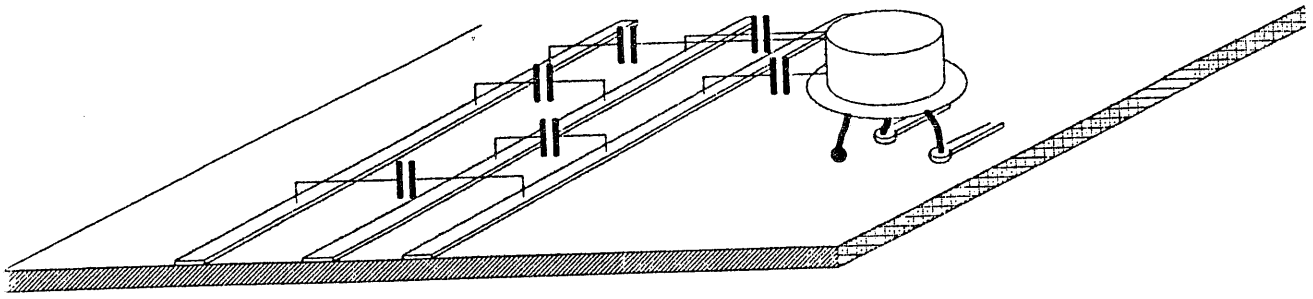


Figure 6 Capacitive coupling between conductors in close proximity

$$V_v = I_v Z_v \quad (2)$$

where V_v is the voltage induced in the victim, I_v is the current induced in the victim as given by Equation (1) and Z_v is the impedance of the victim circuit. This results in higher voltages being introduced into high impedance circuits than into low-impedance circuits. The effect of capacitive coupling may sometimes be reduced by reducing the victim circuit impedance; e.g. by adding additional resistance or capacitance in parallel with the circuit. Clearly this technique can only be used if the increased loading does not affect the circuit performance.

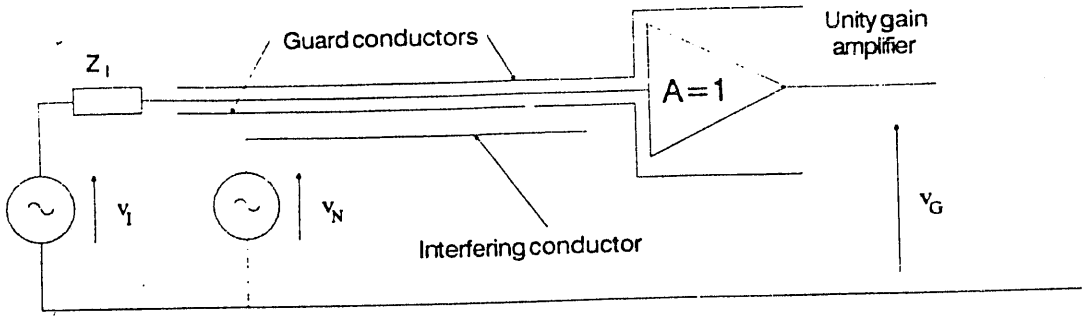
Capacitive coupling can be reduced by several techniques:

a) reduction of the actual coupling capacitance by increasing the separation between the conductors or by reducing the area of overlap;
b) the use of an earthed screen between the conductors to prevent the electric field produced by one from reaching the other;
c) reduction of the coupling effect by using a ground-plane near the conductors;
d) Use of guard conductors to reduce the coupling effect.

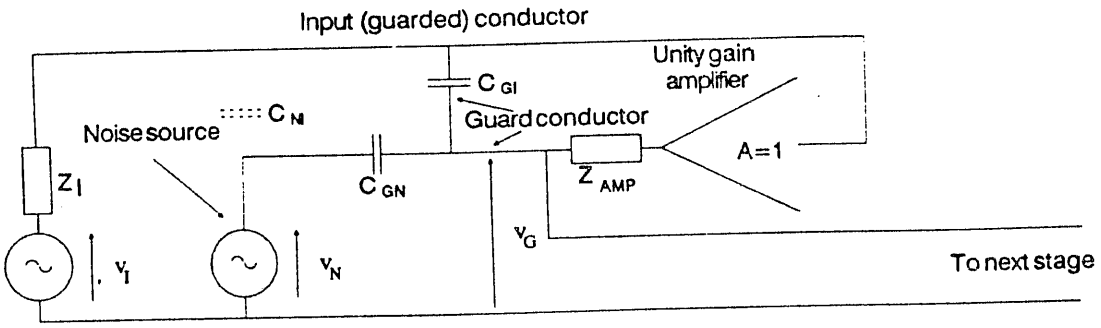
Careful layout of the components on a PCB can be used as a primary measure to reduce coupling capacitances between potential source and victim circuits; i.e. don't run the input track back under the output stage in a high gain amplifier circuit and keep sensitive analogue circuits well away from high power or switching circuits. Where the close proximity of source and victim circuits is necessary then one or more of the remaining techniques must be used. b), c), and d) above all reduce the coupling by altering the electric field pattern around the source so as to reduce its magnitude in the vicinity of the victim. The use of screen and ground planes are considered in section 4.3 and will not be discussed further here.

Guarding is a technique better known for the minimisation of leakage currents in high-impedance instrumentation circuits; the connection from a high impedance source is surrounded by a conductor at the same voltage thus preventing any leakage currents from flowing away from the source conductor. Guarding is usually achieved by driving the guard conductor from the output of a unity gain buffer which is driven from the signal source. The presence of a guard conductor prevents capacitive coupling to the guarded conductor because it is surrounded by an equipotential surface in just the same way as a shielded conductor. The difference between guarding and shielding is due to the fact that the "shield" conductor is kept at the same potential as the shielded conductor rather than at earth potential; this means that the effective capacitance between the guarded conductor and the guard is zero. The shielding effect is achieved and the effective

capacitance of the guarded conductor to ground is reduced to zero. Fig. 7 shows the principle of guarding.

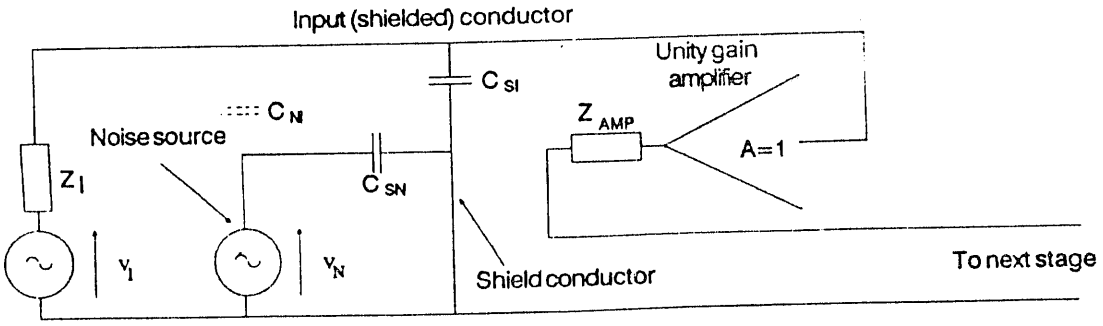


Layout of circuit using guard conductors



Equivalent circuit with guard conductor in use

The placing of the guard conductor between the input and the interference source inherently reduces C_N. If the input conductor is completely surrounded by the guard conductor C_N is effectively zero. If the amplifier output impedance is low compared with the reactances of C_{GI} and C_{GN}, then the voltage across C_{GI} is effectively zero and as well as preventing interference on the input, the guard does not load the input in the same way as an earthed screen would.



Equivalent circuit with grounded shield conductor instead of guard

Figure 7 The use of a guard conductor to reduce capacitive coupling

2.3 Inductive coupling

A magnetic field exists around any current carrying conductor; any change in the current flow produces a proportional change in the magnetic field and this change induces an e.m.f in the conductor itself (self-inductance) and any other nearby conductors (mutual-inductance). Fig. 8 shows the principle of inductive coupling between adjacent conductors.

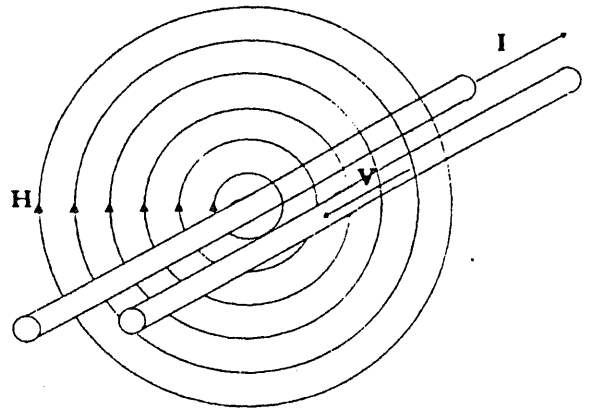


Fig. 8a Inductive coupling between adjacent conductors
(Only one conductor shown carrying current)

$$v_2 = L_2 \frac{d i_2}{dt} + M \frac{d i_1}{dt}$$

$$v_1 = L_1 \frac{d i_1}{dt} + M \frac{d i_2}{dt}$$

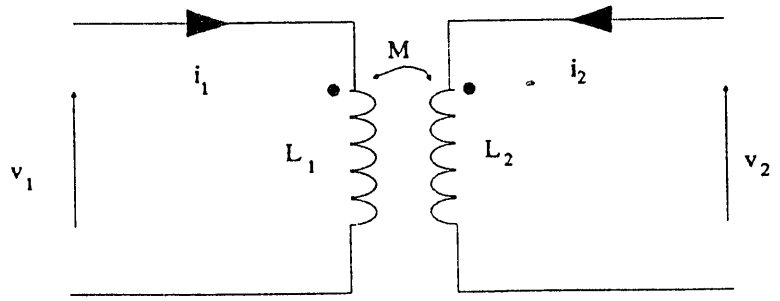


Fig. 8b Equivalent circuit for magnetically coupled conductors

Figure 8a and b

The e.m.f. induced in the victim conductor by a change in current in the source conductor is given by:

$$E_v = M \frac{dI_s}{dt} \qquad (3)$$

where I_s is the current in the source conductor, M is the mutual inductance and t is time. Since the effect of inductive coupling increases with dI/dt, the most likely source circuits are ones in which large or rapidly changing currents are present (e.g. switching regulators, high speed logic circuits, power switching circuits, and power amplifiers). Inductive coupling inherently increases with the frequency of operation of circuits.

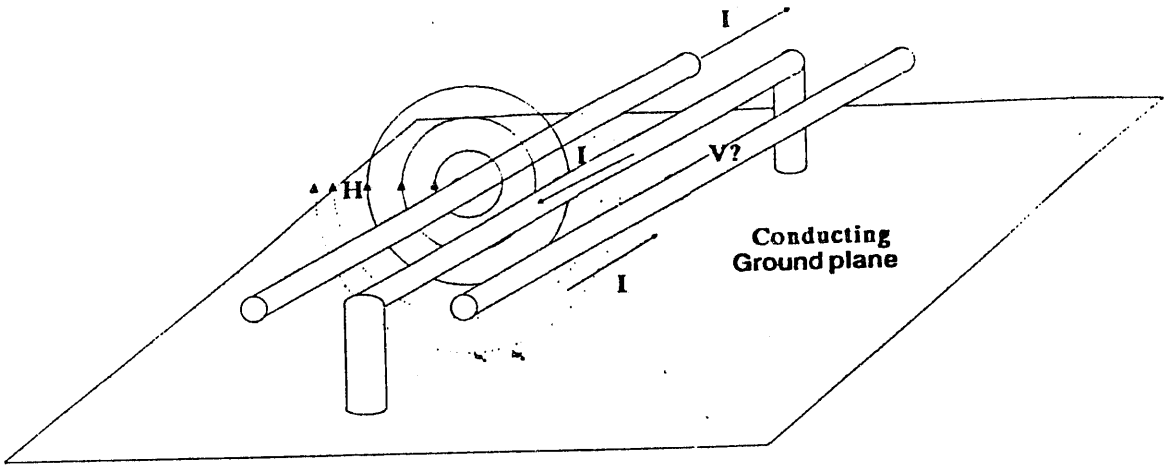


Fig. 9a Inductive coupling between adjacent conductors reduced by conducting shield

$$v_1 = L_1 \frac{di_1}{dt} + M_{12} \frac{di_2}{dt} + M_{13} \frac{di_3}{dt}$$

$$v_2 = L_2 \frac{di_2}{dt} + M_{12} \frac{di_1}{dt} + M_{23} \frac{di_3}{dt}$$

$$0 = L_3 \frac{di_3}{dt} + M_{23} \frac{di_2}{dt} + M_{13} \frac{di_1}{dt}$$

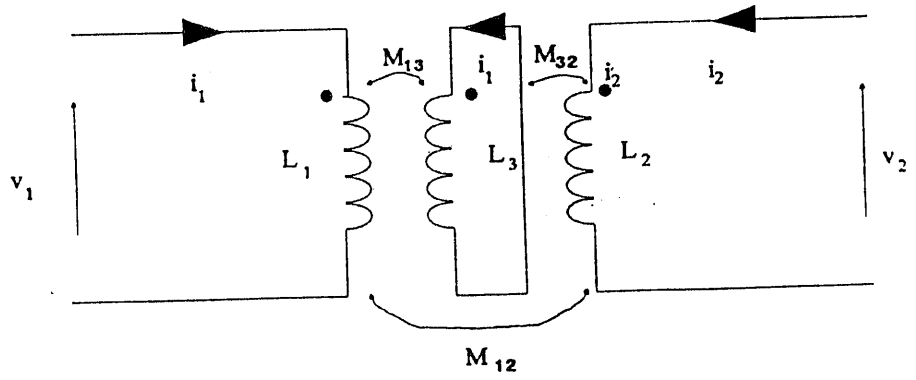


Fig. 9b Equivalent circuit for magnetically coupled conductors with conductive screen

Figure 9a and b

Inductive coupling on PCBs is usually due to long parallel track runs or closely coupled loops. It can be reduced by a number of techniques similar to those used to minimise capacitive coupling:

a) reduction of the mutual inductance between tracks by increasing the separation between the conductors;
b) the use of an earthed screen between the conductors which acts like a shorted turn on a transformer reducing the self- and mutual inductance of the conductors;
c) reduction of the coupling effect by using a ground-plane near the conductors.

It should be noted that it is parallel runs that contribute most to inductive coupling, conductors crossing at right-angles exhibit no mutual inductive coupling.

Screens and ground-planes work by providing a low impedance path in which the induced e.m.f. causes a large current to flow, this induced current produces a magnetic field which tends to cancel that of the source conductor and hence reduces the effect on other nearby conductors (Fig. 9). To be effective the screens must present a low impedance to the induced e.m.f..

2.4 Combined capacitive and inductive coupling

Very often capacitive and inductive coupling are present simultaneously. At frequencies where the track lengths are longer than 1/2 wavelength and the circuits must be considered as transmission lines the effect of combined coupling is to induce a wave in the victim which travels in a direction opposite to that in the source (Fig. 10). The effect of such coupling can be minimised by terminating the affected circuit(s) with its characteristic impedance.

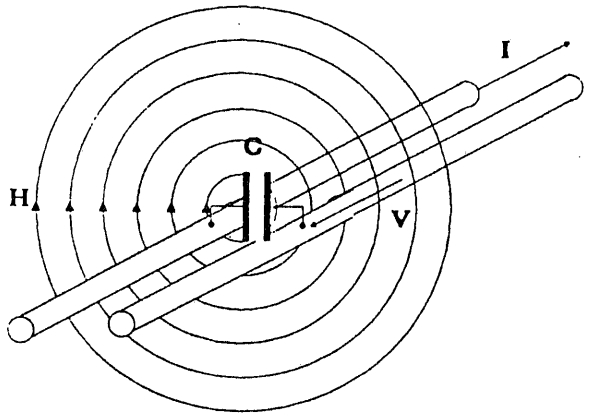


Fig. 10a Inductive and capacitive coupling between adjacent conductors (Only one conductor shown carrying current)

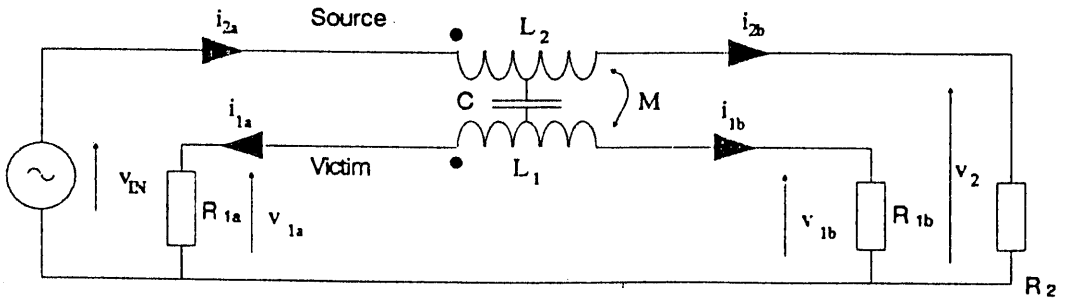


Fig. 10b Equivalent circuit for source and victim with both inductive and capacitive coupling

Figure 10

3 Digital circuits

So far we have considered the possible coupling mechanisms which can cause self-interference on a PCB. It should be also noted that many of the measures which serve to reduce the possibility of self interference also reduce emissions and susceptibility to external interference. In this section effects particular to digital circuits are considered; both susceptibility and sources of interference in digital circuits are considered.

3.1 Noise margins (revision)

One of the most useful characteristics of digital circuits is their ability to completely regenerate a noisy signal provided the level of the noise is below a certain threshold - the noise margin of the circuit. Once the noise level exceeds the circuit noise margin, it is impossible to regenerate the signal. Many factors may contribute to the noise levels within a digital circuit and some noise will be due to external signals but here we only be concerned with on-board noise sources. Some allowance must be made for external noise sources when considering how much noise can be tolerated in the system; internal noise sources must therefore be significantly less than the circuit noise margin.

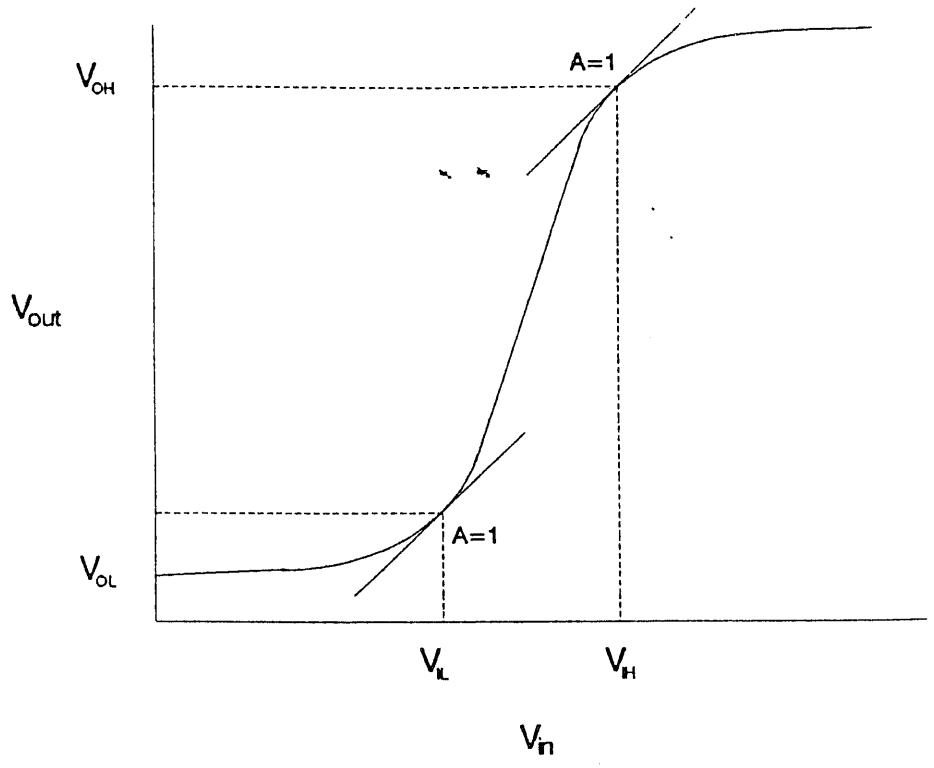


Fig 11 Transfer function of logic gate showing V_{IL}, V_{IH}, V_{OL}, & V_{OH}

Figure 11

3.1.1 D.C. Noise margins

Fig. 11 shows the general transfer characteristic of a logic gate. In order to have the regenerative property mentioned above, the output voltage of a gate must have a high-level which is higher than the minimum high-level required by the input of the next gate and a low-level which is lower than the minimum low-input level required by the next gate. The minimum high- and maximum low-input levels (V_{IH} and V_{IL}) are defined as the points at which the slope of the transfer characteristic passes though one (see Fig. 11). The reason for this definition is that any change in input when $V_{in} > V_{IH}$ or $V_{in} < V_{IL}$ result in a smaller change in output voltage and so, as long as the input voltage is in this range any noise on the input is attenuated as it passes through the gate, and will eventually be reduced to zero. Once the input voltage is in the range $V_{IL} < V_{in} < V_{IH}$ then the slope of the transfer function is greater than one; any noise on the input voltage will therefore be amplified and the regenerative property of the gate will fail. The worst-case output voltages V_{OL} and V_{OH} are defined as the output voltage when $V_{in}=V_{IL}$ and $V_{in}=V_{IH}$ respectively for the non-inverting transfer function shown in Fig. 10. The D.C. noise margins are defined as:

$$NM_L = V_{IL} - V_{OL} \qquad (4)$$

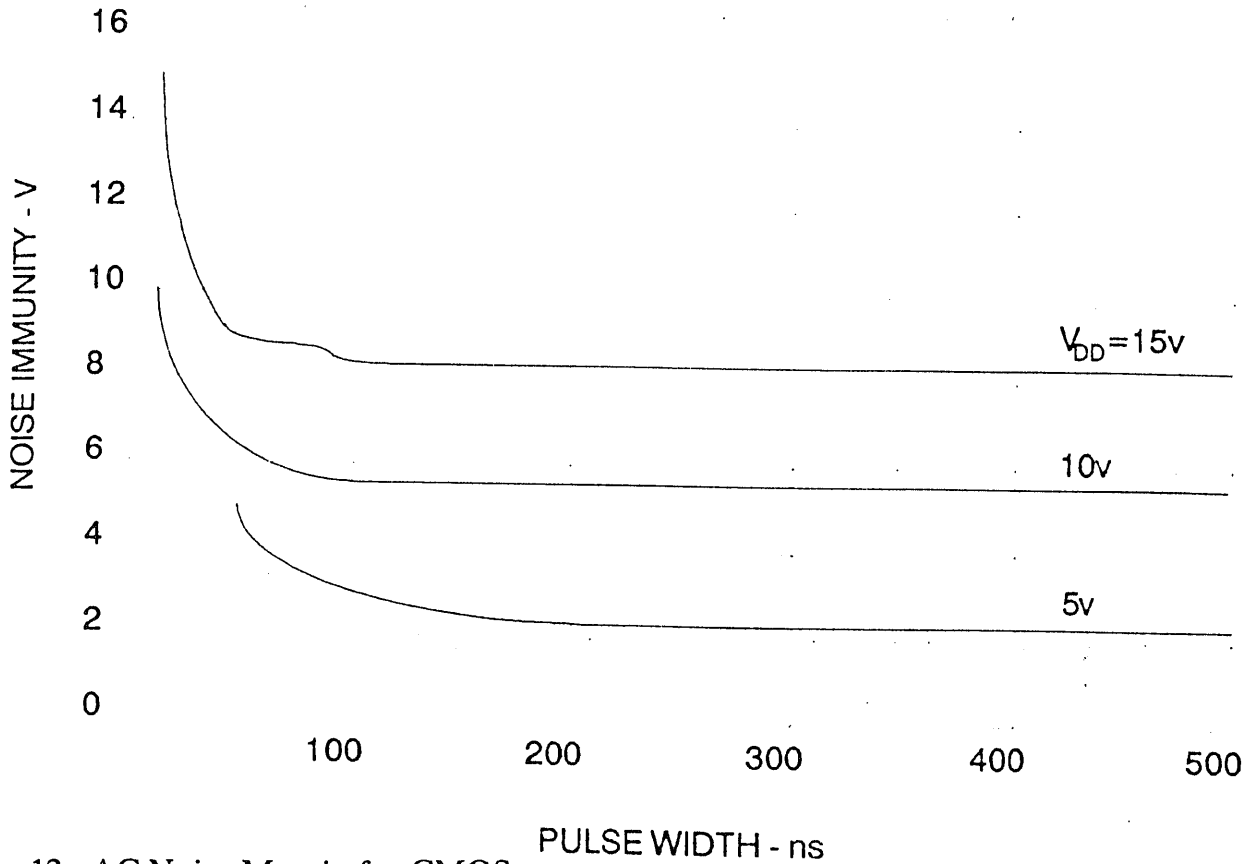
the low noise margin and

$$NM_H = V_{OH} - V_{IH} \quad (5)$$

the high noise margin.

3.1.2 A.C. Noise margins

Due to the finite bandwidth of logic gates their ability to respond to high frequency[1] interference is limited. A very short pulse which exceeds the D.C. noise margins may not affect the output level of the logic gate. The amplitude (above V_{OL} or below V_{OH}) of pulse which may be tolerated for a given short pulse is known as the AC noise margin of the gate and is often given as a graph of pulse amplitude against pulse width in manufacturers application data. Once an interfering pulse becomes shorter than the output rise-time of the gate then the response of the gate is reduced and the D.C. noise margins may safely be exceeded (See Fig. 12).



g 12 AC Noise Margin for CMOS

Figure 12

3.2 Noise Budget

Table 1 over the page shows the D.C. noise margins of popular logic families (worst case margin only). Once the noise margin of the logic family to be used in a design is known then allowances can be allocated for various noise sources and design calculations performed to ensure that the total noise is within the allocated allowance.

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[1]High frequency is used in this context to mean frequencies beyond the bandwidth of the logic gate being considered.

Family	Noise Margin (mV)
TTL	400
LS-TTL	300
S-TTL	300
ALS-TTL	400
FAST-TTL	300
CMOS* (4000B series)	1V
CMOS* (HC)	800
CMOS* (AC)	1.25V
CMOS* (ACT)	700
ECL (10K)	100
ECL (100K)	100

* 5V supply

Table 1 Noise margins of popular logic families

A possible noise budget for a TTL logic circuit is given in Table 2 below. The table indicates each possible noise source and allocates the noise margin evenly between them. Accurate calculations on an arbitrary large system may be difficult or impossible but this simple technique give a basis for some quantitative calculations to be made. If the board layout is well designed then many of the sources of noise can be quantified.

Noise source	% of total	Voltage (mV)
Power supply noise & ripple	20	80
Power & Ground track volt drop	20	80
Data line reflections & ringing	30	120
Cross talk	20	80
External radiation pickup	10	40
Total	100	400

Table 2 Example noise budget for TTL logic circuit

The budget given here is only an example, in any design trade-offs must be made; e.g. if supply and cross-talk is reduced below the levels indicated above a further margin is available for immunity to external interference.

As well as being affected by noise on the gate inputs, changes in supply voltage may also reduce the effective noise margin of the gate and so supply ripple and volt-drops in the power supply lines are normally included in the noise budget for a system. Also any induced noise on the supply lines must also be considered under this heading.

3.3 Power line noise and supply decoupling

Power line noise comes from the three sources given above. Power supply ripple is very much a function of power supply design/selection and is not considered further here; except to say that it is an effect which must be considered.

Volt-drops due to supply track impedances can be estimated and steps taken at the design stage to reduce their effect to a level within the system noise budget. Table 3 below shows the possible switching and load currents taken by simple gates of various logic families. Two figures are given: all types with totem-pole or complementary output stages (not ECL) take a significant transient switching current due to both output transistors conducting simultaneously during switching, this figure is given in the first column; A typical load current for each type of gate is given in the second column, this is a figure which is heavily dependant upon the actual load of the gate. Transient load currents required to drive transmission line or capacitive loads can be far in excess of the D.C. load presented by gates being driven.

Family	Gate Only (mA)	Typical Load (mA)	Switch Time nS
TTL	16	8	10
LS-TTL	8	11	8
S-TTL	30	20	3
ALS-TTL FAST-TTL		11#-60	2
CMOS* (4000B series) 1		1#	>50#
CMOS* (HC)	1	20#	10
CMOS* (AC)	1	8#-100@	<3#
CMOS* (ACT)	1	8#-100@	<3#
ECL (10K)	0	<100@	<2
ECL (100K)	0	<100@	<2

* 5V supply

50pF load

@ Driving 50Ω transmission line

5 gate fanout assumed as minimum load value (maximum value shows worst case load which can be driven).

Table 3 Switching currents for various logic families

Assuming a power supply inductance of 24nH (see Fig. 2) for a well designed PCB and the TTL gate given above switching 24mA in 10ns then the supply rail voltage drop is 57mV which is within the budget figure if negligible voltage drop occurs at the decoupling capacitor (with the poor layout with 210nH track inductance the drop would have been 0.5V, too much!). 10nF of decoupling capacitance per gate would give an extra 10mV drop if all gates switch simultaneously.

3.2.1 Limitations of decoupling capacitors

Careful selection of supply decoupling capacitors must be made for modern high-speed logic circuits. The Schottky TTL families and the new fast CMOS varieties have rise times of 2-3ns. This implies frequency components of well over 100MHz occur in the switching waveforms. Many types of capacitor exhibit self-resonant effects at much lower frequencies (particularly those using wound construction). Also the large dielectric losses of some types (high-K ceramics) mean that the capacitors exhibit larger than expected impedances at high frequencies (above a few MHz for High K ceramics (Class 2 dielectrics)). The leads of a decoupling capacitor can exhibit significant inductance and unless care is taken to keep the length of the leads to a minimum, even the best high frequency capacitor will be significantly handicapped.

Small value (1nF) ceramic capacitors of the temperature compensated type (Class 1) exhibit a good high frequency response but may need to be augmented with larger (0.1F) high-K types and medium sized electrolytic capacitor(s) should be used to provide a further on-board reservoir for low frequency components. Capacitors designed to be mounted under an IC package, which have extremely low self-inductance and good high-frequency performance are available from a number of suppliers.

3.2.2 Use of supply planes and low-Z power buses

For multi-layer PCBs the use of power-supply planes, where a whole layer of the PCB is dedicated to each power supply and return, provides the best power supply performance. The parallel planes have a significant distributed capacitance which is effective at high frequencies and the large area of copper gives a very low resistance. The construction also has a very low self-inductance.

On single- or double-sided PCBs where power supply planes are not possible the use of a single ground plane can greatly improve the circuit performance.

The use of proprietry power supply busses such as described in 2.1 can also greatly improve the power supply distribution on single and double sided boards. The absence of power supply tracks on the board itself can make routing of other tracks much easier.

3.3 Transmission line effects and ringing

When logic gates with very fast rise-times drive long PCB tracks then the tracks must be considered as transmission lines. The propagation velocity on a glass fibre PCB (ε_r=4.7) is about 8in/ns (c/0.7). Once the length of a PCB track becomes of the same order as the length of the rising edge of a logic transition then reflections from unterminated tracks can interfere with the forward signal transition[2].

Even when PCB tracks are short compared with the logic transitions, track inductance and capacitance of the gate inputs and the track can cause high frequency oscillations (ringing) to occur on data transitions.

3.4 Summary of Common logic family characteristics

3.4.1 CMOS 4000 series

A slow, low-power family capable of operation over a wide supply voltage range with very good noise margins. High impedance of circuits makes them more susceptible to external EMI effects than other families although the good noise margin compensates to some extent. The complementary output stage takes significant current pulse when gate switches due to both output transistors being switched on simultaneously. Relatively slow rise-times and small currents mean that this family tend to produce less radiated EMI than other families.

3.4.2 TTL

An old favourite but now largely superseded by the Schottky variants (LS, S, ALS, & F families) and CMOS replacements (H, HCT, AC, & ACT families). Poor (low) noise margins and poor immunity to ground line noise are the main problems. The totem-pole output sinks large supply current pulse as the output switches and both transistors conduct momentarily.

3.4.3 Schottky TTL family (S, LS, ALS, F)

The members of this family exhibit essentially the same characteristics as the basic TTL gates. The trend has been toward faster operation and lower power consumption with increased output drive capability. Schottky (S) TTL was the first member of this family and replaced the old H (High-speed) TTL with slightly lower power consumption and higher speed performance. Low-power Schottky (LS) is the current industry standard, it is slightly faster than standard TTL with about half the power dissipation. The Advanced Low-power Schottky (ALS) and FAST families are a further extension of the line providing a three-fold increase in speed over LS types with similar power consumption. It also has a much greater output drive capability, which is needed for driving transmission line loads and maintaining fast transition times with capacitive loads.

Unfortunately the trend towards increasing speed and output drive capability means that EMC problems become more acute.

3.4.4 The new high speed CMOS families (AC and ACT)

CMOS has finally reached the point where it can out-perform the fastest of the TTL families with very low static power consumption, although the dynamic power consumption equals that of LS-TTL at its upper frequency limit. The ACT series is designed to be directly compatible with TTL gates in circuit and sacrifices some speed and noise immunity to this end. The AC series has improved CMOS level noise margins. All of the gates are designed to be able to drive 50 Ω transmission lines (Better than FAST). Consequently very large currents can flow (100mA/gate) with very fast (3ns) edges. As far as EMC is concerned these gates are the worst yet.

4.4.5 ECL

Traditionally the fastest logic family, the latest versions are just hanging on against CMOS technology. ECL has very small voltage swings compared with TTL and CMOS so even with very fast transition times (<1ns) the dV/dt experienced is similar to the faster TTL/CMOS devices. Commensurate with its small voltage swings ECL also has small noise margins (100mV) but since lines are often terminated and balanced it is not over-sensitive to noise. The large currents required to drive terminated lines means that careful decoupling is required. This may be relaxed somewhat if balanced signals are used. Current flows all the time within the gate resulting in a large static power consumption.

4.4.6 NMOS

This is still the dominant technology for VLSI circuits. The use of depletion-load gates means that NMOS has a much larger static power dissipation than CMOS. The family is relatively slow in operation (similar to or slower than TTL). Logic levels used on external pins are usually TTL compatible and suffer the same limited noise immunity. Outputs have a poor drive capability and are typically capable of driving 1 or 2 standard TTL loads (many more AC or LS loads). This poor drive capability does have the advantage that dV/dt and output current during switching is low. A typical VLSI circuit may take a considerable fraction of an amp supply current so power supply impedance is important.

4 Analogue circuits

Although the EMI mechanisms are the same for all circuits, different sources and effects are observed in analogue systems to those found in digital systems.

4.1 Effects of external EMI on analogue circuits

Here the term external means from sources other than the circuit itself: e.g. other circuits on the same PCB or from off-board sources.
Although EMI is categorised below into different regions in the frequency domain, broad-band signals may have frequency components which extend across the boundaries given and more than one effect may be present.

4.1.1 Interference in circuit normal-signal pass-band

The normal-signal pass-band is the frequency range which the normal input signal occupies, which may be different from the pass-band of the circuit itself. The main problem with interference in the normal signal pass-band is that it cannot easily be removed by filtering of signal connections.

Interference in the circuit pass-band is processed in the same way as the normal signal. The effect in many circuits is simply one of increasing the noise level at the output of the circuit, particularly if the interference is broad-band in nature. In this case the acceptable level of interference depends upon the acceptable signal-to-noise ratio (SNR) at the system output and the effects of interference are entirely predictable.

With some circuits, such as phase-locked loops (PLLs), narrow-band interference may cause complete breakdown of normal circuit behaviour; i.e. the PLL may lock onto the interfering signal rather than the local signal.

A further effect is that of shorts, high amplitude interference pulses, such as those caused by switching transients, which may cause the circuit to become overloaded. Many analogue circuits, particularly those with inductive or capacitive elements in a feedback loop, take a considerable period to recover from an overload condition. Thus the effect of the interference on the wanted signal may be much greater than is apparent from its short duration. Apart from minimising the actual interference level, the effect of this type of interference may be minimised by limiting the allowable voltage swing at critical points in the circuit to that of the normal signal. This will minimise the effect of overload conditions by ensuring that the overload energy stored in inductors and capacitors in the circuit does not exceed that for normal signal levels. Fig. 13 shows an

example of such an application. An integrator circuit is used to process the output of a magnetic tape head in a magnetic-card reader system. The output of the magnetic pickup is the derivative of the magnetic flux pattern on the card; the output of the integrator is therefore proportional to the flux pattern on the card irrespective of the swipe speed. A pre-amplifier is required before the integrator to prevent it loading the tape-lead output and to allow convenient component values to be used in the integrator. Although the signal from the card reader varies with the speed at which the card is manually swiped through the reader its output is a maximum of about 20mV. A pre-amplifier with a voltage gain of 10 is adequate for this application giving a 200mV input to the integrator. The integrator is designed to give a 2Vpk-pk output swing with the normal card flux-density. This output drives a comparator with hysterisis which is used to produce a signal at logic levels for decoding of the digital data stored on the card. This design has poor immunity to pulse noise because the pulse can be amplified through the system and become much bigger than the normal signal before it reaches the integrator. The integrator can fully integrate the pulse without overload to give a maximum output of +/-15V, this is much larger than the normal signal and consequently, even with the leaky-integrator design shown the circuit may take many bit-periods of the digital input signal to recover from a noise pulse. The effect of an interference pulse could be greatly reduced by the inclusion of the amplitude limiting circuitry shown dotted on the circuit diagram.

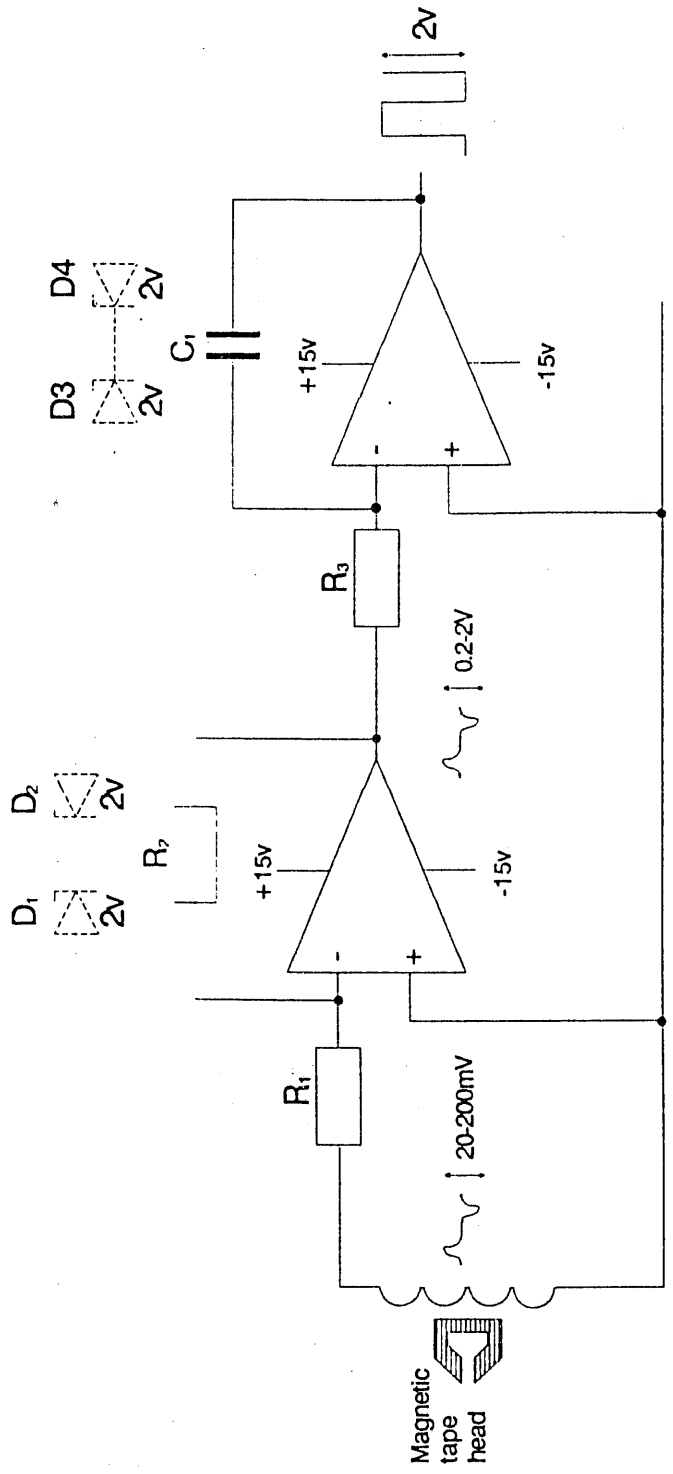

Fig 13 Improving pulse noise immunity in analogue circuits

Figure 13

4.1.2 Interference outside normal-signal pass-band but inside circuit pass-band

The effect of this type of interference is essentially the same as described in 4.1.1. The important difference is that this type of interference can be avoided by reduction of the circuit bandwidth to

that of the normal signal. This can easily be forgotten when designing with modern IC building blocks which often have circuit bandwidths well in excess of that required for common uses.

4.1.3 Interference outside circuit pass-band

Interfering signals outside of the pass-band of a circuit can still have a significant effect on circuit operation although the sensitivity of the circuit is likely[2] to be much lower than for in-band signals. The effects of this type of interference are due to its interaction with the non-linearities which are present in all active devices (including rectifiers, zener diodes etc.). Three effects occur: rectification of the interfering signal which can disturb the D.C. bias levels in the circuit; the generation of intermodulation products with the wanted and other interfering signals, which may be within the circuit pass-band; and generation of harmonics of the interfering signal which are within the circuit pass-band.

Passive filter circuits must be used to eliminate this type of interference when it may enter the circuit by conduction. Effective screening is the only way to eliminate pickup of radiated interference (including capacitive and inductive pickup).

4.2 Self-interference in analogue circuits

Unwanted coupling between different parts of an analogue circuit often results in oscillatory behaviour; whilst this is readily observable, it only indicates when a significant degree of coupling is present, smaller amounts of coupling may have an adverse effect upon system performance. A circuit which is just on the threshold of self-oscillation may behave as a tuned amplifier for frequencies at or near the natural frequency of oscillation. This means that the circuit is likely to be very susceptible to external EMI at this frequency.

5 Concluding remarks

There is no substitute for a well designed layout to reduce the danger of unwanted coupling, but the layout of PCBs is often left to draughtsmen with little or no knowledge of these effects. Design engineers must consider the effects of layout on their designs and pass on guidelines to the PCB draughtsman as to likely critical areas. Very often a few guidelines as to where to place components and how to route signal and power supply tracks given to the draughtsman can alleviate any potential problems before they occur. One problem with choice of layout and routing is that the best layout is often not the easiest to produce; many on-board EMC problems are caused by taking the easiest route.

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[2]See 8.4.2, the effect of unintentional regenerative feedback may greatly increase the sensitivity of a circuit to signals outside the normal pass-band.

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