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A DIGITAL POWER AMPLIFIER USING SWITCHED-MODE POWER SUPPLIES

J.P. Atherton

Department of Electrical & Electronic Engineering, Bolton Institute of Higher Education, Deane Road, Bolton BL3 5AB

ABSTRACT

This paper describes the use of multiple switched-mode power supplies (SMPS) to create a power amplifier. Its primary use is when the signal is already in digital form, such as replaying from digital tape, when it may be considered as a power digital to analogue converter. The SMPS's are programmed by the digital words, held in a buffer store, in advance of being switched to the loudspeaker by high power field effect transistors (MOSFETS).

1. INTRODUCTION

The advent of digital techniques in audio systems has resulted in a considerable amount of research and investment in the last decade or two but the area of digital power amplification has lagged somewhat behind. There are a number of technical reasons for this outlined, along with consumer's fashionable interest, by Sandler[1]. The development of a truly digital power amplifier which is of the form of a high power digital to analogue converter (D/A) would have many technical advantages over a conventional linear power amplifier since designers of the latter have to make many compromises in areas such as bias circuits for stability/distortion tradeoffs.

Power MOSFETs are now available with very low on resistance, high current capabilities and fast turn-on and turn-off times. This paper outlines the multiplexing of high currents directly into a loudspeaker at the digital data rate. The currents are obtained from programmable switched-mode power supplies which have been programmed, by the audio signal, a few samples before they are required.

Digital audio after error correcting, de-interleaving etc., is held in a buffer store and clocked out at the sample rate t_s (e.g. 48 KHz). In principle these data words could program an SMPS which is connected to the loudspeaker but a pulse width modulated (pwm) SMPS would, for 16 bit resolution, have to have an internal clock which counted through 2^{16} states in one cycle. If the frequency of the SMPS were 250KHz this would imply an unrealisable clock rate of 16GHz. Another factor is the settling time of the SMPS which, although improving is still too long.

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Two techniques to alleviate these problems are outlined in this paper. The first is that since a number of sample words are available in the buffer state of the audio source, they can be accessed and each used to set up an SMPS so that it may settle by the time the word is needed.
The second technique is that of considering the audio word (1 sign bit + 15 magnitude bits) as two 8 bit words each programming an SMPS, in a 'coarse' + 'fine' adjustment. The two SMPS's are then algebraically summed. This has the effect of reducing the clock rate required. For example, 8 bit resolution at a repetition rate of 250KHz would require a clock rate of 64MHz.

2. BASIC SYSTEM OUTLINE

The principle of operation is outlined in Fig. 1 which shows the samples in the buffer store and the multiplexing of the SMPS outputs. At time t=0 SMPS A is outputting sample 1 to the loudspeaker and samples 2 and 3 are already setting up SMPS B and C. At the next sample time, t_s, sample 2 from SMPS B is switched to the loudspeaker and sample 4 loaded into SMPS A. At $2t_s$ sample 3 is switched to the loudspeaker and sample 5 loaded into SMPS B and so on. There is therefore two sample periods for an SMPS to settle before it is required to output its voltage.
The loading of the SMPS pwm counters and the multiplexing of the outputs are under the control of the system sampling clock. The multiplexing into the loudspeaker is accomplished by power field effect transistors (MOSFETs). In practice a set of both positive and negative SMPS's are used in conjunction with the sign bit of the audio word.
Since all power supplies regulate to some extent when on load and voltage loss will occur due to the on resistance of the MOSFET an error will occur between the analogue representation of the digital word and the actual voltage obtained. This is corrected by converting (at high speed) the analogue output to a digital word, comparing it with the word held in the buffer and applying a correction to the counter in the SMPS. This feedback loop is shown in Fig. 2 and is only operative for any particular SMPS at the time of outputting a sample. This is the reason for the multiplexer on the output of the A/D converter. During the other sample periods the SMPS is open loop.

3. SWITCHED-MODE POWER SUPPLIES

As mentioned in Section 1, an SMPS with a conventional pulse width modulator operating with a 16 bit word length requires an impractically high internal clock frequency. Any digital

word, however, may be considered as the sum of two words (with appropriate weighting) so the most significant 7 magnitude bits can set a 'coarse' SMPS and the least significant 8 bits set a 'fine' SMPS, (see Fig. 3). These operations may be done concurrently and the internal clock generators and counters then operate at a speed realisable by current logic families (e.g. fast CMOS or ECL). Each SMPS shown in Fig. 1 therefore comprises two SMPS's connected in series as shown in Fig. 4. The input voltages Vin_1 and Vin_2 are of course common to all SMPS's of that polarity and their value is dictated by the power required into the load. To relate this to a specific example consider the case of 100W required into an 8Ω load. A peak load voltage of 40V is required so the most significant magnitude bit must represent ½ full scale and Vin_1 must be 40V. The 'coarse' supply therefore has a resolution of 312.5mV and Vin_2 must be 312.5mV as shown in Fig.5.
In principle the word length may be broken down into 3 or more sections with a consequential lowering of clock rates even further, or alternatively achieving higher precision by increasing the word length whilst keeping the clock rate of the pwm's the same.

4. DISCUSSION

This paper has presented one form of power D/A converter for use as a loudspeaker drive amplifier. There is no requirement for the digital audio to be converted to analogue form then linearly amplified. The use of multiple SMPS's does have disadvantages of cost and size but as they improve, particularly in the areas of speed and settling time, their numbers may be reduced. In principle the system may be extended to "look ahead" any number of samples and investigations are in progress to compare digital words for a number of subsequent samples and determine when the 'coarse' power supply needs changing. As this is likely to be less often than the 'fine' power supply it may be possible to have, say, two 'coarse' supplies and multiplex the 'fine' supplies. Switched-mode power supplies currently have efficiencies of around 80-90% so the method holds promise for efficient very high power amplifiers which are thermally stable.

5. REFERENCES

[1] M. SANDLER, 'Techniques for digital power amplification', Proc. Reproduced Sound 3, p.177, Inst. of Acoustics, 1987.

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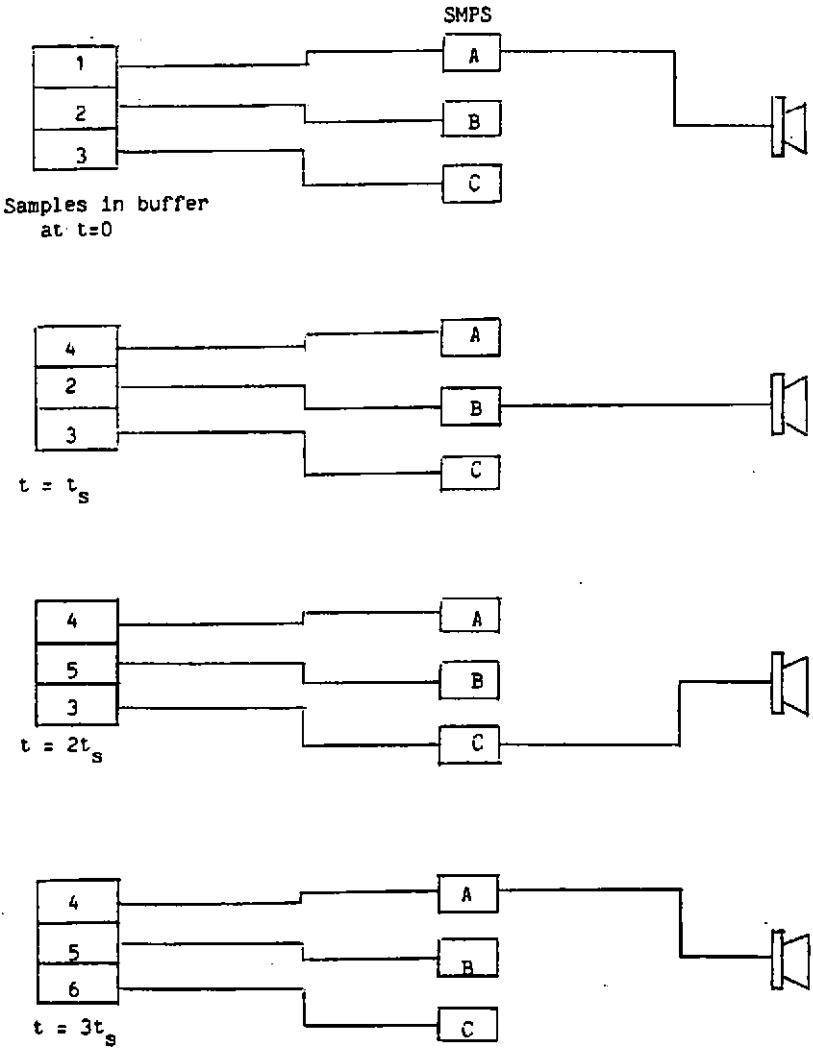

Fig. 1 Principle of System Multiplexing

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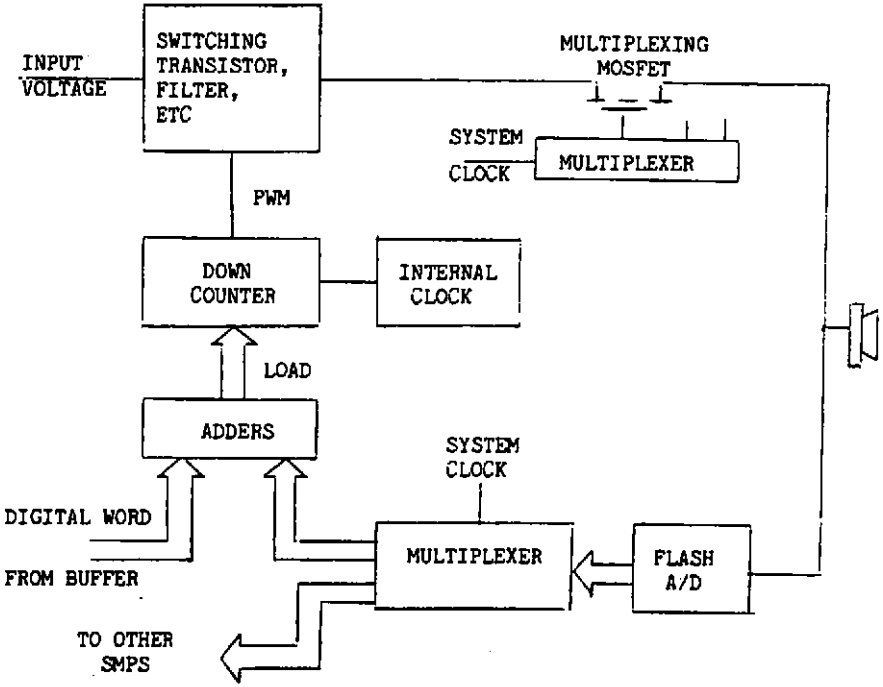

Fig. 2 Multiplexed feedback loop

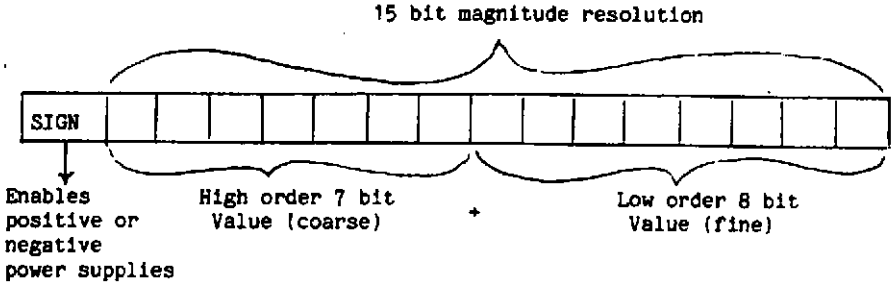

Fig. 3 Digital word as two bytes

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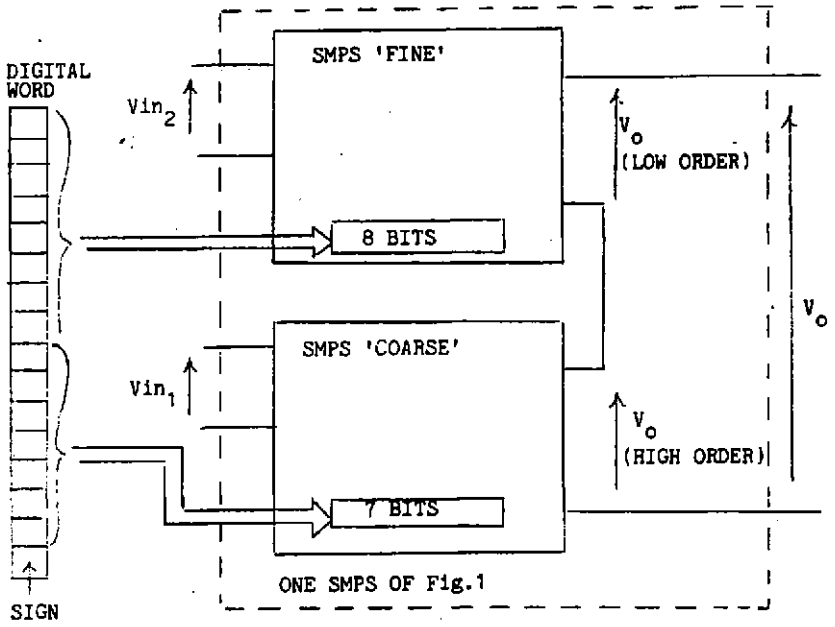

Fig. 4 Connection of 'coarse' and 'fine' SMPS's

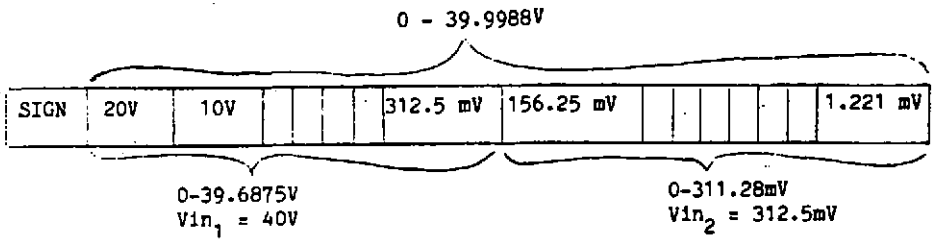

Fig. 5 Specific voltages for 100W into 8Ω