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Tandem quadruplet VCA topology

M. O. J. Hawksford, University of Essex

0 Introduction

Voltage controlled amplifiers currently find a wide application in professional audio systems [1] where they function as remote controlled gain elements and a means of achieving programmable, parametric equalization. Most modern devices are based upon bipolar transistors [2 to 6] where the key element is the base emitter I_E/V_{BE} characteristic which for an ideal device adheres to the law,

$$V_{BE} = \frac{k\,T}{q} \ln\left[\frac{I_E}{I_S}\right] \qquad \ldots 1$$

where
- V_{BE}, base emitter voltage
- I_E, emitter current, ampere
- k, Boltzmann's constant, 1.38E-23 joule/kelvin
- T, absolute temperature, kelvin
- q, charge on electron, 1.602E-19 coulomb
- I_S, saturation current, ampere

VCA cells operate with matched transistors using either pairs or quadruplet arrays. Cells based upon pair matching, where the two series V_{BE} voltages add and are equated to a constant gain control voltage, produce a logarithmic gain law, while a 4 transistor cell where $\sum V_{BE} = 0$ produce a linear gain law with lower temperature sensitivity. Also, the incorporation of complementary working, offer significant topological advantage, by easing the design with respect to bias current absorption and also reducing the number of amplifiers required to both condition the input voltage and derive the output voltage, especially when operating in a single-ended mode as opposed to differential working.

In this paper, we explore a new cell topology based upon the complementary emitter follower configuration, where the parallel connection of base emitter junctions of NPN/PNP transistors can yield a near constant slope impedance with signal current over the class A operating range and can be programmed by modulating the cell bias current. Also, by cascading a number of such cells in series, the input voltage can be fully developed across silicon junctions without recourse to potential division via a resistor, as such higher signal to noise ratios are possible that do not require the adoption of class AB biassing together with the associated problem distortion and modulation noise, there is also lower sensitivity to noise in the biasing circuitry.

1 Parallel, complementary basis cell

The basis cell of the new VCA system is shown in Figure 1 and consists of a

voltage bias source V_B, and two complementary transistors T_1, T_2 configured in an emitter follower mode where, including the bias voltages, the base emitter junctions are effectively in parallel. We define v_c as the instantaneous voltage across the cell, i_c the output current and $I_B + i_c/2$, $I_B - i_c/2$ as the respective, instantaneous currents in T_1 and T_2. Although the signal current distribution between T_1 and T_2 is shown as symmetrical, the current I_B may also include a common mode component and thus effectively change with signal level from its quiescent value (ie $i_c = 0$) of I_{BO}. The cell transconductance is defined,

$$g_m = \frac{\partial i_c}{\partial v_c}$$

where our aim is to seek the best condition for constancy of g_m to enable the cell to be exercised over a maximum signal space. In passing, we note that the cell input current is effectively zero and that although the collector currents of T_1, T_2 include dynamic biasing (that is, $I_B = f(i_c)$), that the difference of the collector currents is equal to i_c.

System equations

applying Kirchhoff,

$$v_c = - V_B + V_{BE1}$$

$$v_c = V_B - V_{BE2}$$

and from equation 1,

$$V_{BE1} = \frac{k\,T}{q} \ln\left[I_B + \frac{i_c}{2}\right]$$

$$V_{BE2} = \frac{k\,T}{q} \ln\left[I_B - \frac{i_c}{2}\right]$$

where assuming transistors T_1, T_2 are matched thermally and parametrically

$$2\,v_c = \frac{k\,T}{q} \ln\left[\frac{I_B + i_c/2}{I_B - i_c/2}\right] \qquad \ldots 3$$

$$\text{and } 2\,V_B = \frac{k\,T}{q} \ln\left[\frac{I_B^2 - i_c^2/4}{I_s^2}\right] \qquad \ldots 4$$

Forming the derivative $\partial i_c/\partial V_c$ from equation 3 and noting the definition for g_m in equation 2.

$$g_m = \frac{qI_B}{kT}\left[\frac{1 - \left(\frac{i_c}{2I_B}\right)^2}{1 - \frac{i_c}{I_B}\frac{\partial I_B}{\partial i_c}}\right] \quad \ldots 5$$

To explore the behaviour of g_m with i_c, consider the following biasing methods:

(i) Constant voltage biasing, V_B = constant

Consider the cell bias voltage V_B to be constant, where in equation 4, $\partial V_B/\partial i_c = 0$ which yields $\partial I_B/\partial i_c = 0.25 i_c/I_B$, thus equation 5 gives,

$$g_m = \frac{2q}{kT} I_B$$

However, assuming constant V_B and $I_B = I_{BO}$ when $i_c = 0$, then from equation 4, $I_B^2 - (i_c/2)^2 = I_{BO}^2$, giving

$$g_m = \frac{2q}{kT} I_{BO}(1 + (i_c/(2I_{BO}))^2)^{0.5}$$

If we define the quiescent transconductance (that is at $i_c = 0$) as g_{mo},

$$g_{mo} = \frac{2q}{kT} I_{BO} \quad \ldots 6$$

and a loading factor x as,

$$x = \frac{i_c}{2I_{BO}} \quad \ldots 7$$

$$g_m = g_{mo}(1 + x^2)^{0.5}$$

(ii) Constant current biasing, $I_B = I_{BO}$

Constant current biasing (that is I_B remains independant of i_c) can be achieved using the bias circuit in Figure 2 where diodes D_1, D_2 have identical characteristics to transistors T_1, T_2 and are thermally matched; this also has the desirable characteristic of eliminating the thermal dependence on I_s and T as expressed in equation 4. Assume that the diodes are driven by differential currents $I_{BO} + i_c/2$, $I_{BO} - i_c/2$, whereby

$$V_B = \frac{k\,T}{q} \ln \left[\frac{I_{BO}^2 - i_c^2/4}{I_s^2} \right]$$

hence equating with V_B from equation 4, $I_B = I_{BO}$. Since I_B is now constant, $\partial I_B / \partial i_c = 0$, where from equation 5, 6 and 7

$$g_m = g_{mo} \left(1 - x^2\right)$$

Once more the cell exhibits non linearity, but a comparison with g_m for constant voltage biasing, now shows the distortion is in the opposite sense.

(iii) Intermediate biasing

The findings in (i) and (ii) suggest a more optimum performance by seeking an intermediate biasing condition between the two extrema, hence we modify the current drive in Figure 2 to $I_{BO} + \alpha\, i_c/2$, $I_{BO} - \alpha\, i_c/2$ where α is a constant, giving

$$V_B = \frac{k\,T}{q} \ln \left[\frac{I_{BO}^2 - \left(\alpha\, i_c/2\right)^2}{I_S^2} \right]$$

then again equating V_B with equation 4,

$$I_B^2 = I_{BO}^2 - (1 - \alpha^2)\,(i_c/2)^2$$

Differentiating and substituting into equation 7, observing the definition of equation 6, 7 yields

$$g_m = g_{mo}(1 - \alpha^2 x^2)(1 + (1 - \alpha^2)x^2)^{1/2} \qquad 8$$

This result is a compromise solution between the constant voltage and constant current bias modes, where for illustration, we define a distortion factor $D(x, \alpha)$,

$$g_m = g_{mo}(1 + D(x, \alpha))$$

whereby,

$$D(x, \alpha) = (1 - \alpha^2 x^2)(1 + (1 - \alpha^2)x^2)^{1/2} - 1 \qquad \ldots 9$$

In Figure 3, a family of $D(x, \alpha)$ is plotted against x ranging from 0 to 1 and α ranging from 0.5 to 0.6 in steps of 0.05, where acceptable linearity is demonstrated for $\alpha = 0.65$.

2 Error correction for transistor bulk resistance

VCA cells that use bipolar transistors require the individual devices to adhere to an accurate logarithmic relationship where the transistor should exhibit good *logarithmic conformity*. Appropriate transistor selection and choice of bias

currents together with the minimisation of signal dependent changes in collector to base voltage (to eliminate contributions from slope impedances) can improve logarithmic conformity, although the ohmic voltage drops associated with emitter and base bulk resistances set an ultimate bound on performance. The effect of bulk resistances can be represented by modifying equation 1 as follows

$$V_{BE} = \frac{kT}{q} \ln\left[\frac{I_E}{I_S}\right] + I_E\left[r_{ee'} + \frac{r_{bb'}}{1+\beta}\right] \qquad \ldots 10$$

where the base bulk resistances $r_{bb'}$ can be reflected to the emitter using the I_C / I_B current gain β and combined with the emitter bulk resistance $r_{ee'}$ to form a composite resistance r_{bk},

$$r_{bk} = r_{ee'} + \frac{r_{bb'}}{1+\beta} \qquad \ldots 11$$

The key to correction for the effects of bulk resistance [6] is to introduce a voltage proportional to emitter current that is appropriately scaled and of opposite polarity to the internal ohmic voltage drops.

8 transistor error correction cell

The basic cell of Figure 1 can be modified by introducing a further 2 transistors in series with T_1, T_2 and then compounding this structure with a similar cascaded circuit as shown in Figure 4. If we neglect the contribution from base currents and assume all transistors to be matched, then for top half of circuit,

$$v_c + 2V_B - V_{BE1} - 2\left(I_B + \frac{i_c}{2}\right) r_{bk} - V_{BE3} - \left(I_B - \frac{i_c}{2}\right) r_x$$

$$+ \left(I_B + \frac{i_c}{2}\right) r_x + V_{BE7} + 2\left(I_B - \frac{i_c}{2}\right) r_{bk} + V_{BE5} - 2V_B = v_c$$

hence if, $r_x = 2\,r_{bk}$ and $V_{BE1} = V_{BE3}$, $V_{BE5} = V_{BE7}$

then $v_c = V_{BE1} - V_{BE5}$

a similar analysis can be performed for the lower half of the circuit where the optimum selection of r_x can again desensitise performance to the contribution of bulk resistance. The bias voltages V_B are multiplied by 2, but the circuit of Figure 2 is readily modified to accommodate this factor.

3 Tandem connection of follower cells

Section 1 and 2 have demonstrate the means by which a complementary follower configuration can be approximately linearized to have a near constant transconductance with signal current, where defining a current I_{BO} in a bias circuit with signal current, voltage V_B can be produced which determines the cell transconductance to be proportional to the current I_{BO}.

However, as with all bipolar cells, the input voltage range is restricted which implies a limitation in signal to noise ratio (SNR). In this section we investigate a tandem connection where a number of cells N are connected in cascade such that each cell sees only a fraction of the total input voltage, which can now be of greater level. A basic structure is shown in Figure 5 where N pairs of cells are used. The input signal V_{in} is divided by an equi-value resistor network to produce intermediate voltages to which are added the appropriate bias voltages V_B using unity-gain summing amplifiers. We may therefore assume that with appropriate transistor matching, that the resistance of each cell r_c is identical and that each carries a nominal signal current i_c. A positive attribute of this configuration is the insensitivity to noise components appearing on the intermediate driving nodes of each quadruplet, as signals at these nodes introduce equal and opposite signal currents in adjacent cells such that when currents are summed, the differential errors cancel. Thus, the noise contribution of each intermediate unity-gain amplifier introduced between resistor divider networks and each cell is minimised.

Signal to noise ratio

Assume that each cell can accommodate a peak signal level $\hat{v}_c$ where $\hat{v}_c = I_{BO}/g_{mo} = kT/q$, (≈ 25mV) before the onset of unacceptable distortion, and that at a particular state of bias, the total cell noise source has a mean square value $\overline{e_c^2}$ in series with the cell resistance r_c (where $r_c = 1/g_m$).

$$\therefore \text{ Peak SNR (1 cell)} = \left(\frac{\hat{v}_c}{r_c}\right)^2 \left(\frac{r_c^2}{\overline{e_c^2}}\right) = \frac{\hat{v}_c^2}{\overline{e_c^2}}$$

If there are N cells in series, the peak input voltage is now $N\hat{V}_c$ and if all cell currents are summed, the peak signal current is $N\hat{V}_c/r_c$. However, the components of noise currents add on a *power basis*, therefore

$$\text{mean square noise current} = N\frac{\overline{e_c^2}}{r_c^2}$$

whereby, the total SNR becomes

$$SNR_{(N\ cells)} = N\frac{\hat{v}_c^2}{\overline{e_c^2}}$$

However, there is an upper bound to the number of cascaded cells that is determined by the peak input signal $\hat{V}_{in}$, where

$$N_{opt} = \text{int}\left[\frac{\hat{v}_{in}}{\hat{v}_c}\right]$$

If the optimum number N_{opt} is exceeded, then the loading on each cell is correspondingly reduced, reducing both distortion *and* SNR. It is also expedient to compare the performance of the cascaded cell structure with that of a parallel connection of N cells as shown in Figure 6. In fact, both cell configurations will offer potentially the *same* SNR providing we assume the associated biasing sources and amplifiers to be noiseless. However, when we introduce noise sources into the biasing amplifiers (that includes the noise from V_B), then the following points should be noted:

(i) In the parallel connection, each cell sees the same external noise source developed across the cell resistance r_c, therefore through coherent addition and the effective system resistance r_c/N, the external noise sources undergo significant amplification.

(ii) In the series connection, the outputs of the intermediate amplifier ($x_2, x_3, x_4; y_2, y_3, y_4$) when summed via the individual assumed identical cells, cancel as any two adjacent amplifiers are driven in an opposite sense by the noise component $\dot{e}_n$.

(iii) In the series connection, it is only the external noise sources presented at the nodes x_1, x_5 and y_1, y_5 which contribute to a net output current, but these are produced across an effective resistance r_c of the first cell and similarly for the N^{th} cell.

(iv) In the series connection, although the intermediate voltages do not contribute directly to the output, they are necessary to steer each cell into its optimum operating range to minimise distortion.

4 Conclusion

The paper has introduced a quadruplet cell that functions similarly to an emitter follower. A theoretical study demonstrated that by using an optimized, dynamic biasing system that the complementary NPN/PNP parallel connection of transistor could yield improved linearity compared with either constant voltage or constant current biasing. The cell offers a linear gain law where transconductance is directly proportional to a current I_{BO} applied to the bias circuit, which also offers the advantage of a low temperature sensitivity providing the cells use matched transistors under isothermal operation.

A tandem connection of identical cells was shown to give an improved SNR and offer (compared with a parallel connection) lower sensitivity to noise in associated amplifiers and bias circuits. Although the present paper has not presented complete circuitry, the system approach introduced sufficient detail to demonstrate the feasibility of a VCA using the follower cell, where in particular the role of error correction for ohmic voltage drops in the bulk resistance of transistor was discussed thus allowing each transistor to achieve more accurate logarithmic conformity. Similarly, when implementing a cell, circuitry should be used to maintain both a low and a constant collector base voltage and thus minimise distortion products from transistor slope impedances.

References

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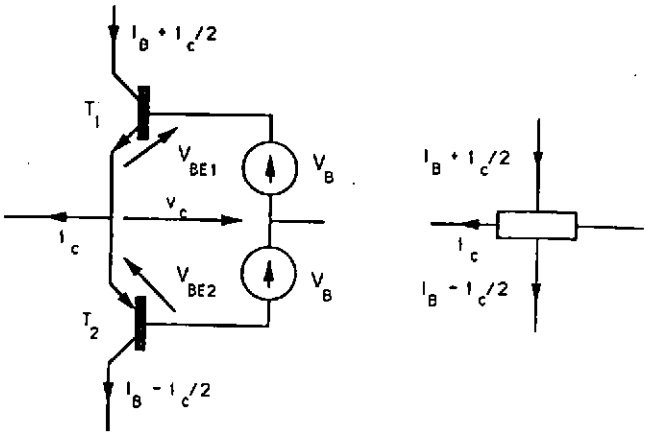

Fig. 1 Basic cell formed from complementary emitter follower

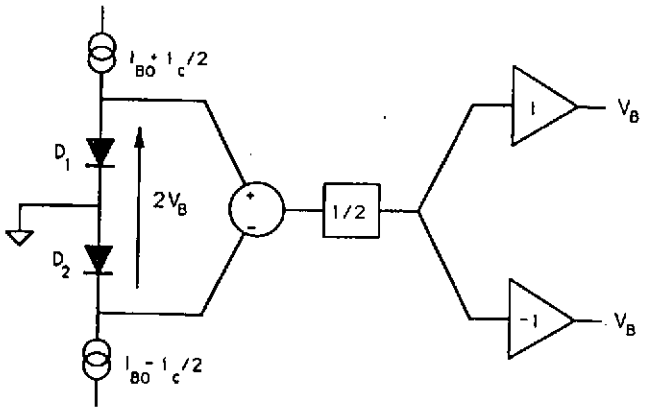

Fig. 2 Derivation of dynamic bias voltage, V_B.

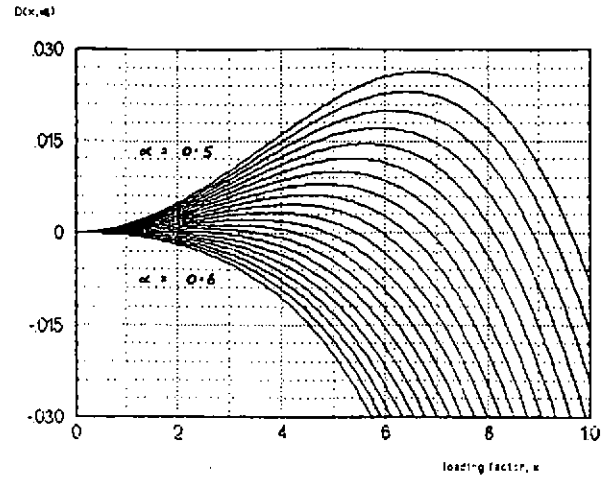

Fig 3 Family of distortion plots D(x,α) against cell loading factor, x; for α = 0.5 to 0.6 in steps of 0.05.

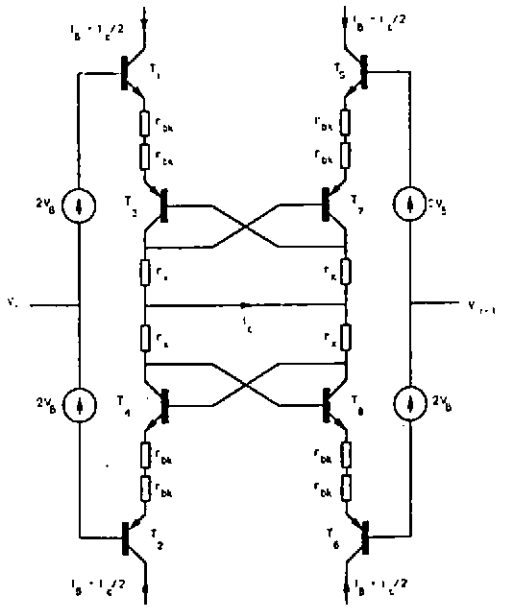

Fig 4 Cascaded cell with error correction to compensate for base and emitter bulk resistance.

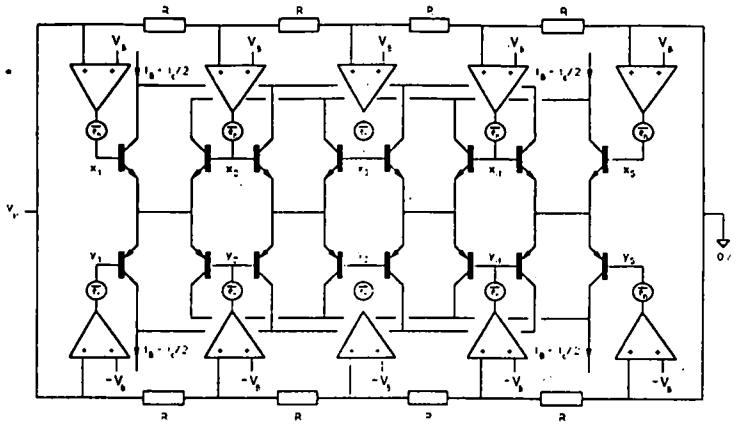

Fig. 5 Series connection of 4 quadruplet gain cells.

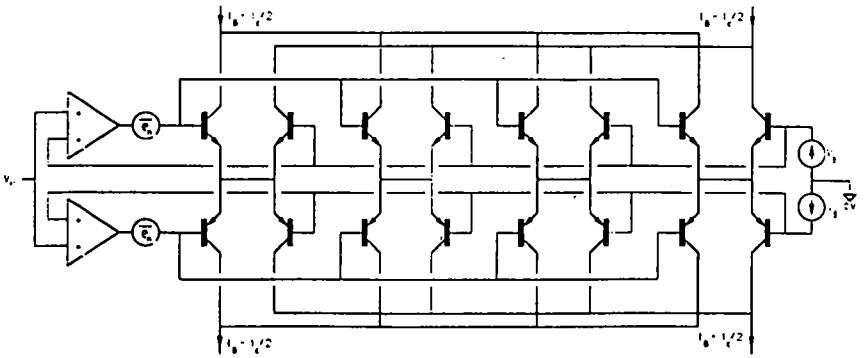

Fig. 6 Parallel connection of 4 quadruplet gain cells.