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AN APPLICATION OF DIRECT MEMORY ACCESS DATA TRANSFERS

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This paper describes a versatile digital sampling system which may be used in many areas of acoustic research.

This system has three prime models of operation; (a) transient recorder, (b) a waveform generator and (c) digital delay line. Primarily it is intended to interface with a minicomputer, which will issue commands under program control over an RS232 serial line. Data transfers will be accomplished by means of a high speed parallel interface. A typical command string could consist of: initiate transient recording, transfer data over parallel interface, reload data after performing desired transformations and finally initiate signal generator to playback the calculated response.

The serial interface may be connected directly to a terminal and the commands issued from there. This type of control is well suited to the delay line mode of operation. When using the delay lines to model dominant room echoes, the length of the delays can quickly be altered from the terminal, thus changing the model characteristics. The serial line can also be connected via a cassette interface to provide additional data storage.

Finally the system can operate in 'stand alone' mode. A limited subset of commands are provided as front panel push buttons, enabling the system to operate without need of a computer or terminal, useful for field measurements. A prerecorded fixed command string could be loaded from the cassette interface should the required operation exceed the capability of the front panel.

The three modes of operation are described briefly below.

(i) The transient recorder will store up to 8192 digitized samples of an analogue signal, (or 4096 samples in stereo) at a sampling rate which is variable from 4 kHz to 256 kHz. A software and a hardware trigger are provided to either start or stop the record cycle.

A 12 bit system was chosen as a compromise between speed and noise. The analogue to digital (A/D) converter can resolve down to 1 bit in 2^{12}, which gives a quantization noise level of -72 dB. To go for higher resolution would reduce the maximum sampling rate of 256 kHz, which will allow detection of 2 kHz 'real' signals in 80th scale models.

(ii) The signal generator can be loaded from the serial line or parallel lines, from a computer or other such data source (cassette, multi track tape, disc...) It would be interesting to compare the speed of these two operations. For the serial line each byte of data (there are two bytes per A/D converter word) is converted into two ASCII hex characters, and inserted into a

formatted line containing addresses, checksum, data type etc. If all 8192 words were to be transmitted, this would require 40,000 ASCII characters, or 400,000 bits. At a data rate of 1200 baud this gives a transmission time of 5 minutes. Under parallel transfer two savings in time are made; firstly a 40 fold saving as each clock pulse takes one word, as opposed to one bit of a character, secondly this transfer is done under DMA control so the data rate is not locked to the throughput rate of the microprocessor. The maximum rate for clocking data into the computer is 20 kHz, thus 8192 words will be transmitted in just under half a second. A considerable saving, especially if an experiment requires many data transfers.

Applications of the signal generator include:
(1) predistorting signals for system excitation, e.g. removing nonlinearities in loud speaker testing.

(2) Periodic excitation with a known signal (e.g. a swept sine wave) to overcome the low power inherent in impulse testing, the phase of successive cycles can be accurately locked through the triggering mechanisms.

(iii) In the delay line operation an analogue signal is digitized and stored in the currently addressed memory location, after the memory has completed one cycle this digital information is read out and passed to a digital to analogue (D/A) convertor. The analogue signal is thus delayed by NxT seconds, where N is the number of cycles per memory cycle and T is sampling period. The delay can also be expressed as N/(2xsignal bandwidth). For a speech signal with 8 kHz bandwidth this gives a maximum delay in the order of 0.5 second. The two channels can be set up with differing delays by altering the number of samples per memory cycle within each channel, the sampling rate of both channels will be the same.

These requirements combine to give a system which is shown in Figure 1.

Methods of storing digitized data

The use of 12 bit data words together with an 8 bit microprocessor presented certain design problems. Under normal operation the micro must transfer each data word in two stages, the least significant 8 bits first followed by the most significant 4 bits. The processor cannot move this data directly from the A/D to the memory, instead all data transfers must pass through the accumulator in the processor. The minimum time required for this two byte transfer under program control is 35 μs. The equivalent sampling rate of <30 kHz is fine for speech analysis, just acceptable for music, but well below the speed required for scale model analysis. The sampling rate for the delay lines will come down to half the above rate; since there are two read/write cycles.

To increase speed DMA is used, in which 12 bit data can pass directly from A/D to memory without the need for a central (8 bit) accumulator. All the necessary timing signals and addresses are provided from within the DMA controller. The only limit on speed now becomes the state of the art in A/D and memory design, in this case a sampling rate of 256 kHz for a 12 bit A/D.

AN APPLICATION OF DIRECT MEMORY ACCESS DATA TRANSFERS

The memory interface circuitry posed some problems as it has to communicate data to an 8 bit processor bus, the dual 12 bit analogue converter bus and the 16 bit parallel bus. Additionally there are two sets of addresses, control and read/write lines, one from the processor and one from the DMA controller. The key signal is DMA ON. When high the processor cannot access the data memory and the DMA buses are selected, when low the processor bus is selected.

In order to get the 12 bit data onto the 8 bit processor bus the data is interlaced, with 8 bit data and 4 bit data on adjacent addresses, thus one memory address is equivalent to two processor addresses.

The DMA controller provides addresses, timing and control signals to enable the direct transfer of 12 bit data between memory and the analogue convertors. The main features are:

(1) Programmable address counters
(2) Programmable clock
(3) Control register

These are programmed from the microprocessor bus and provide a full range of control for the system. The address counters contain the number of samples per memory cycle, and the programmable clock sets up the sampling rate. Any function of the sampling system may be described as an 8 bit byte and loaded into the control register for execution.

Taking a closer look at the timing in Figure 2 shows five important signals during the three modes of system operation.

(1) $\overline{\text{Clock}}$: The memory is enabled when this signal is low
(2) Addresses: These increment on the positive edge of the clock, allowing a settling time before memory is enabled
(3) R/$\overline{\text{W}}$: This signal is low to write data into memory during transient record, high to read data from memory in signal generator mode, and toggles from read to write when memory is enabled to accomplish delay line operation
(4) A/D convert: A negative edge will initiate an A/D convertion, this occurs at the positive edge of $\overline{\text{CLOCK}}$ in transient record, allowing time to ensure data is valid when memory is enabled at the negative edge of $\overline{\text{CLOCK}}$.
5) D/A convert: A positive edge will latch data into the D/A converter, this occurs on the positive edge of $\overline{\text{CLOCK}}$ in the signal generator mode, which ensures valid data, in the delay line it occurs just prior to the R/$\overline{\text{W}}$ line going low, thus previous data is read out of memory before new data is written in.

AN APPLICATION OF DIRECT MEMORY ACCESS DATA TRANSFERS

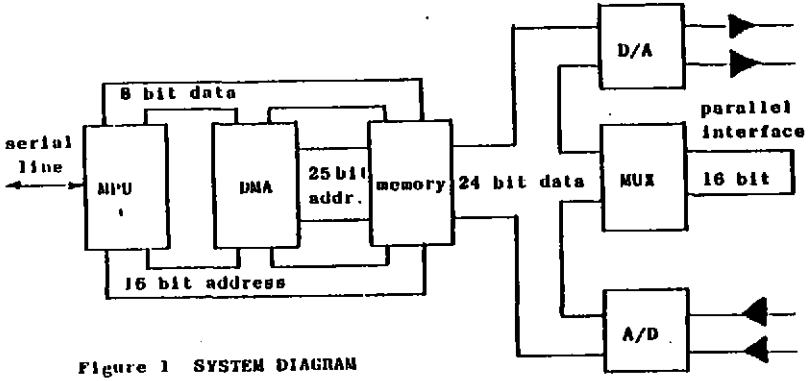

Figure 1 SYSTEM DIAGRAM

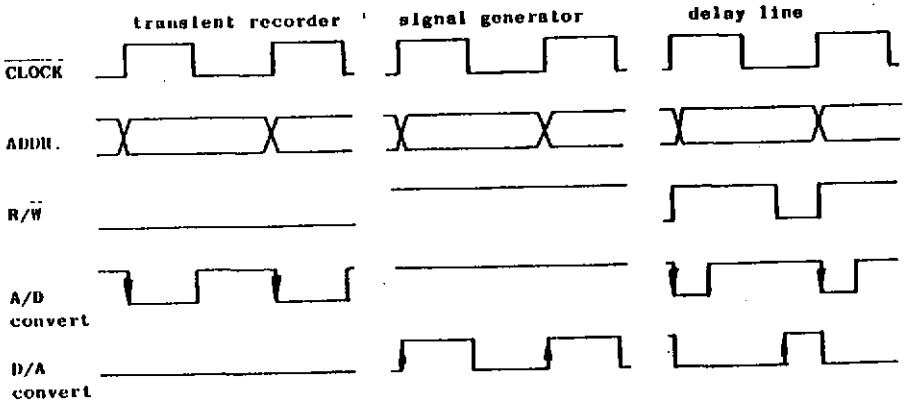

Figure 2 TIMING DIAGRAMS