Proceedings of The Institute of Acoustics 3A14

REAL-TIME, SPECTRAL ANALYSIS OF SPEECH

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1. INTRODUCTION

This contribution describes the implementation, in hardware, of a digital filter bank which is capable of realising 128 band pass filters in real-time. The machine has been designed as a fast 'front end' for a speech recognition system. The output spectra thus become inputs to a computer which will be programmed to perform some kind of feature extraction and recognition. An important facility of the proposed system will be its ability to feedback information from the computer to the spectral processor, to change the filter bank characteristics to suit the nature of the incoming signal. Fig. 1 illustrates the arrangement.

2. SYSTEM OPERATION

The input signal is sampled at 10 KHz and converted to digital format. After digital filtering, the 128 filtered signals are rectified, smoothed and then resampled at a slower rate. These outputs are then compressed in amplitude by taking logarithms. The output from the machine is thus a spectrum consisting of 128 log. amplitude, frequency points. A complete spectral frame becomes available every T seconds, where T is variable, by remote switching, from 3.2m Sec. to 12.8 mS.

The centre frequencies and bandwidths of the filters are determined by a set of filter coefficients stored in P.R.O.M. type memory. This memory holds 8 different sets of coefficients and it is possible to select any particular set by remote switching.

3. FILTER CHARACTERISTICS

Each digital filter is a realisation of the second order sampled data filter

$$\frac{V_o(n)}{V_1(n)} = \frac{a_o(1 - Z^{-2})}{1 + b_1 Z^{-1} + b_2 Z^{-2}}$$

where $V_1(n)$ and $V_o(n)$ are the input and output samples, a_o, b_1 and b_2 are the filter coefficients, and Z^{-1} is the unit sample delay.

The filter coefficients, a_o, b_1 and b_2 are derived from a prototype analogue filter via the bilinear Z-transform. In this method, there is a direct relationship between a_o and b_2, in fact $b_2 = 1 - 2a_o$. Using this, and expanding the above expression, the present filter output sample $V_o(n)$ can be computed from

$$V_o(n) = a_o\left[V_1(n) - Z^{-2} V_1(n) + 2Z^{-2} V_o(n)\right] - b_1 Z^{-1} V_o(n) - Z^{-2} V_o(n)$$

where $V_1(n) Z^{-2} \rightarrow V_1(n-2)$

$V_o(n) Z^{-2} \rightarrow V_o(n-2)$

and $V_o(n) Z^{-1} \rightarrow V_o(n-1)$

The algorithm for digital filtering is thus a simple summation of weighted values of past and present inputs, and past outputs. Only two coefficients and only two non-integer multiplications are required per filter. The frequency response of this type of filter is shown in Fig. 2.

After filtering, the filter outputs are rectified by taking the modulus. Smoothing is accomplished by averaging each rectified output over N samples. Resampling is then at a rate reduced by the factor N, which is variable between 32 and 128. The digital data at this stage consists of 28 bit binary numbers. (This size of digital word is necessary to accommodate the dynamic range). The logarithm generator uses the first 12 non-zero bits of these numbers to give 8 bit log. amplitude output spectra.

4. HARDWARE

For the initiated, a brief description of the hardware. A 12 x 12 bit digital multiplier chip is used with digital shifters to implement a 24 bit floating point multiplier - the heart of the processor. Multiply time is about 150 n Sec. The main accumulator, registers and processing memory are all TTL. The filter coefficient memory is U.V. erasable E.P.R.O.M. Averaging of the outputs is accomplished in a second, 28 bit accumulator. The logarithms are generated by using digital shifters to shift the 28 bit outputs a maximum of 16 places, this gives the first four log. bits. The other four bits are derived from the first 12 bits of the shifted number via a look-up table.

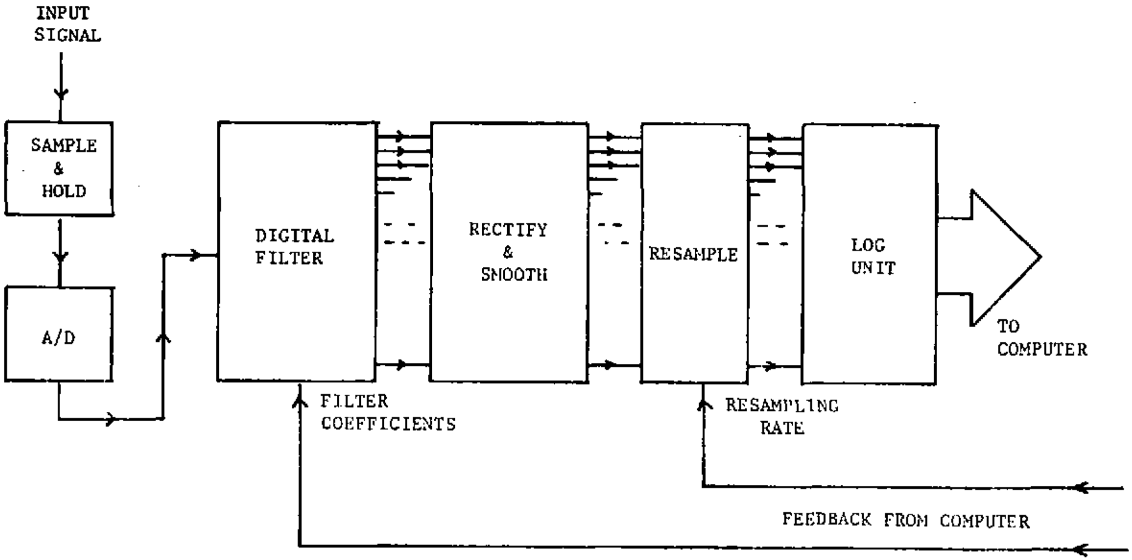

FIG. 1 ADAPTIVE, REAL-TIME SPECTRAL ANALYSER

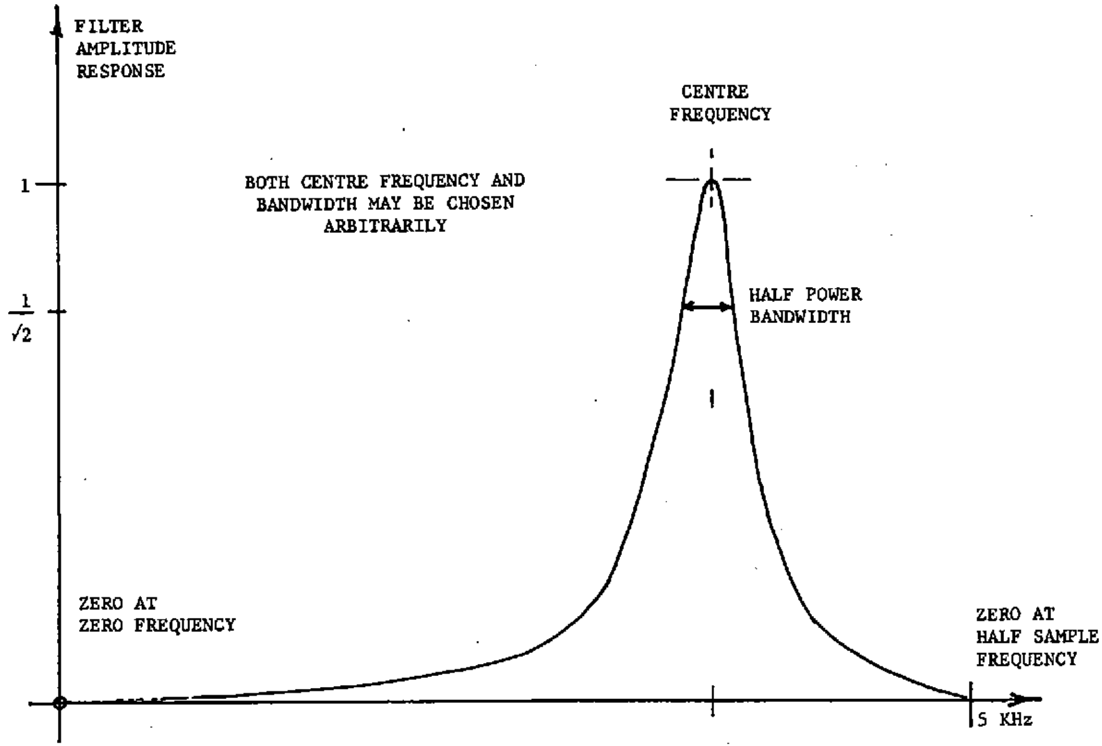

FIG. 2 SHAPE OF TYPICAL DIGITAL FILTER AMPLITUDE RESPONSE