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THE PLATFORM DESIGN FOR ANVC BASED ON KEY-STONE

Tianhao Cui
Institute of Acoustics, Chinese Academy of Sciences, Beijing, China
Email: cth@mail.ioa.ac.cn

Jiahuan Cheng
Institute of Acoustics, Chinese Academy of Sciences, Beijing, China

Multi-core processor can enable a highly efficient active noise and vibration control system. This paper presents a novel design and implementation based on TI's 66AK2H14 DSP. This DSP platform consists of three main parts: multi-core part, A/D part, and power part. The multi-core part includes three components of 66AK2H14, 4GB DD4RAM and 512MB flash as well. The A/D part consists of one FPGA, A/D convertors. The A/D convertor, with a sample speed up to 4Msps, has eight signal input channels each of which is equipped with an analogy multi-band filter. Then the FPGA can carry out eight-channel digital filtering in parallel. This generic DSP platform has been applied in real-world multi-channel active noise and vibration control. The results have reported that the proposed platform can well meet the required processing speed and accuracy for most applications.

1. Introduction

In order to detect, analyze and reduce noise and vibration, more and more perfection systems have been realized base on strong hardware systems architected by multi cores with high processing speed. This paper introduces a perfection system design that has been implemented on TI's 66AK2H14 equipped with eight DSP cores and four ARM cores. The overall block diagram is shown in Figure 1.

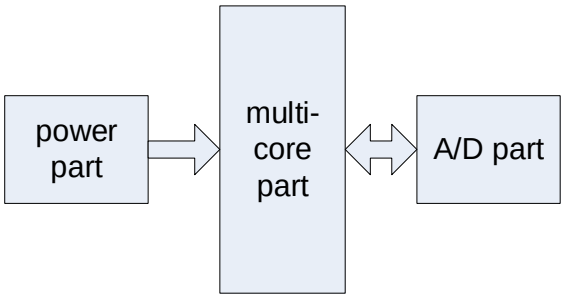

Figure 1: The overview of design framework

This system consists of three main parts: multi-core part, A/D part, and power part.

As Figure 1 shows, analogy signal is input into the A/D part, where it is processed by analogy filter and converted to digital signal. Once digital signals arrive in FPGA which is included in A/D part, the digital signals are processed to match the format of 66AK2H14's EMIF16 peripheral interface in the multi-core part. The multi-core part functions for FFT analysis, communication with Ethernet and USB etc. The power part provides power supply for all parts of the system.

2. A/D part

The A/D part consists of eight A/D Converters module TI's ADS8422, eight analogy anti-alias filter channels and one FPGA module Altera's EP3C80F484. The A/D part block diagram is shown in Figure 2.

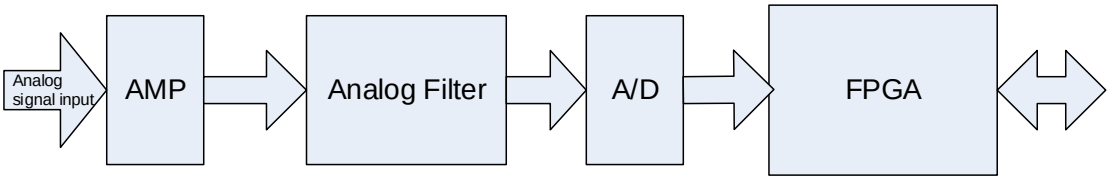

Figure 2: The diagram of A/D part

First, the analogy signal is input into AMP in order to get enhancement. The input signal can been either constant current signal or constant voltage signal which can be flexibly setup by a switch. Next, an analogy filter is used to block high frequency band. Each anti-alias filter channel is built by two amplifiers and one monolithic instrumentation amplifier. The latter works for converting single-signal to diff-signal. In order to achieve good performance, this anti-alias filter is realized by 4th active low pass Butterworth filter. The passband can been flexibly setup. In our design, 1KHz bandwidth is configured as shown in Figure 3.

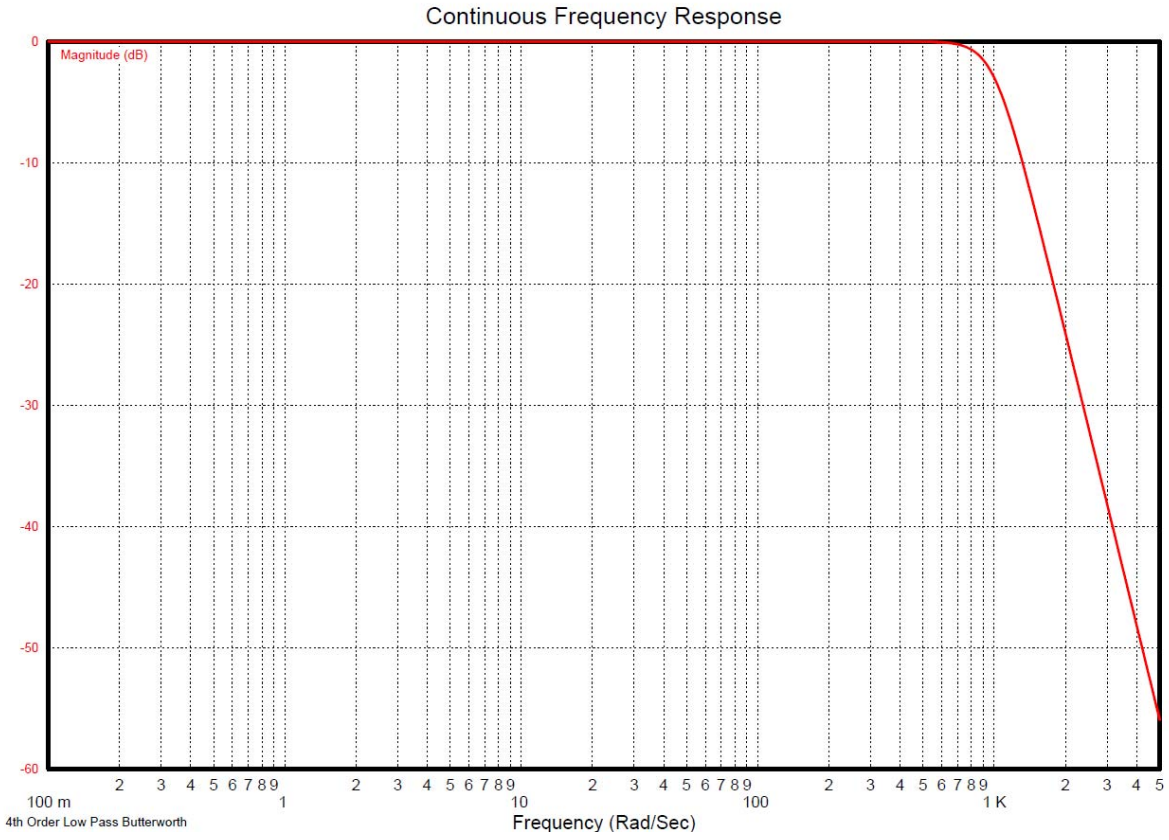

Figure 3: 1K Hz bandwidth

As block diagram shown in Figure 4, the ADS8422 is a 16-bit, 4-MHz sample A/D converter with an internal 4.096-V reference. The device includes a 16-bit capacitor-based multi-bit SAR A/D converter with inherent sample and hold. This converter includes a full 16-bit interface and an 8-bit option where data is read using two 8-bit read cycles if necessary. The ADS8422 has a fully differential, pseudo-bipolar input.

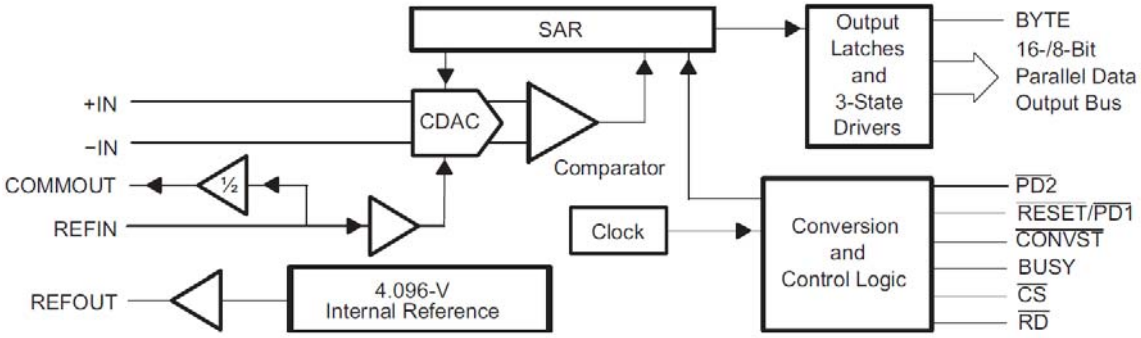

Figure 4. The block diagram of ADS8422

As Figure 2 shows, a FPGA module EP3C80F484 is in this part, to receive data from ADS8422. Then it transmits data to 66AK2H14 via EMIF16 peripheral interface. The FPGA offers a unique combination of high performance, low power and low cost.

3. Multi-core part

The multi-core part consists of one 66AK2H14, 2GB ddr3-1333 SDRAM, 4Gb NAND FLASH and tow SGMII net port. The multi-core part block diagram is shown in Figure 5.

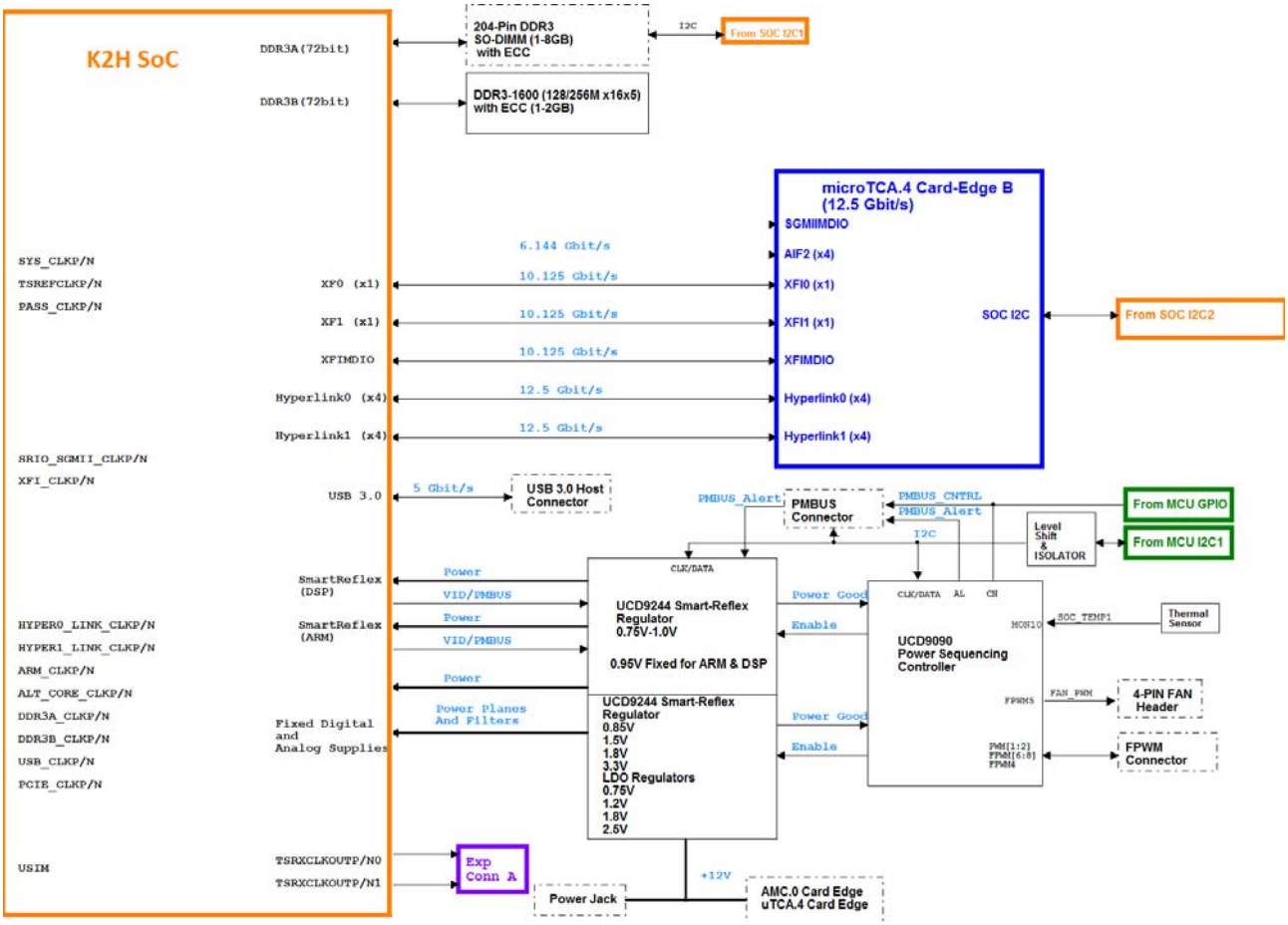

Figure 5 The multi-core part block diagram

The DSP Core subsystems has eight TMS320C66x, where each DSP Core runs on 1.2GHz. The ARM Core subsystems has four Cortex-A15 cores, running on 1.4GHz. Both subsystems share memory and peripheral I/O. This system has four high speed peripheral interfaces: one PCIE interface with speed of 5Gbps which can been configured as host or terminal; one USB3.0 port with speed up to 5Gbps; one HyperLink for companion device interface which is a four-lane SerDes interface operating at up to 10 Gbps per lane from pin-to-pin; and one EMIF16 peripheral interface connecting the device and external memory such as NAND/NOR flash. In the system, the EMIF16 interface is designed to make connection between 66AK2H14 and FPGA which is configured as an external memory device. The redraw wave of TI's development tool CCS from data is shown in Figure 6.

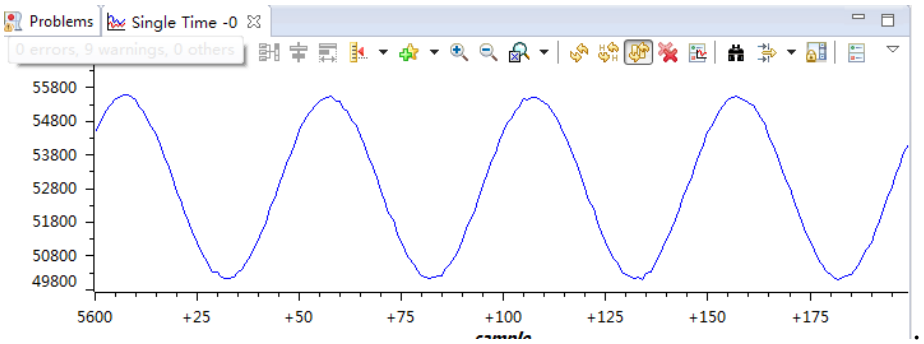

Figure 6: The redraw wave by CCS

4. Power part

The Power Part provides power supply for all other parts of the system. In order to achieve low noise and isolation between A/D Part and Multi-core Part, two separate power supply sources are designed. The power part diagram is depicted in Figure 7

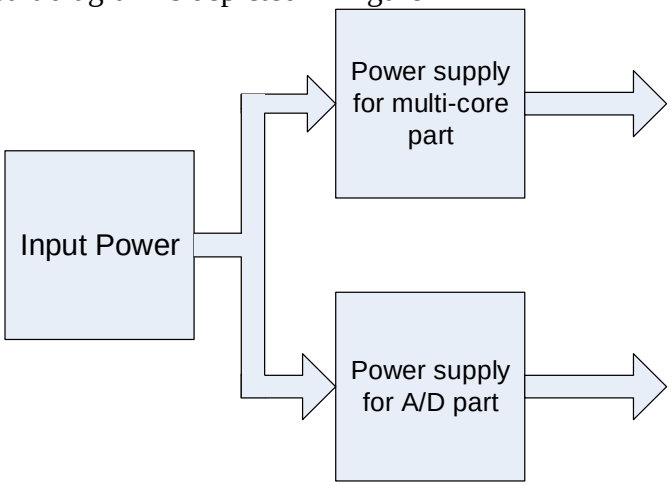

Figure 7. The power part diagram

5. Experimental results

Figure 8, 9 and 10 show the testing results.

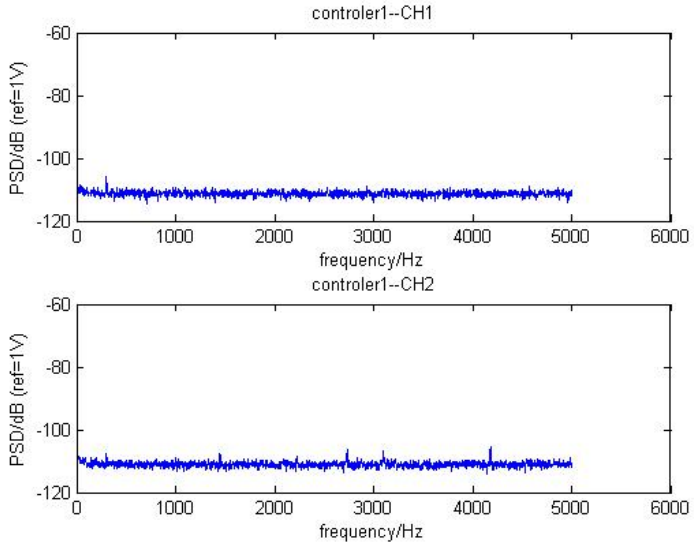

Figure 8: The ground noise of input channel

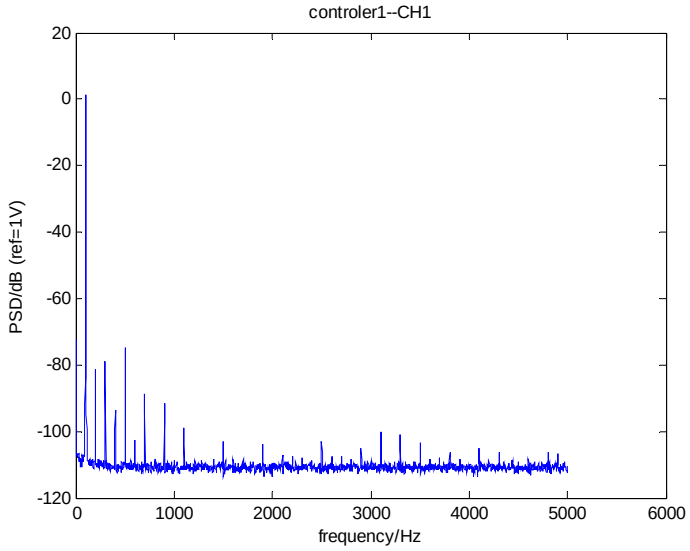

Figure 9: THD of input channel

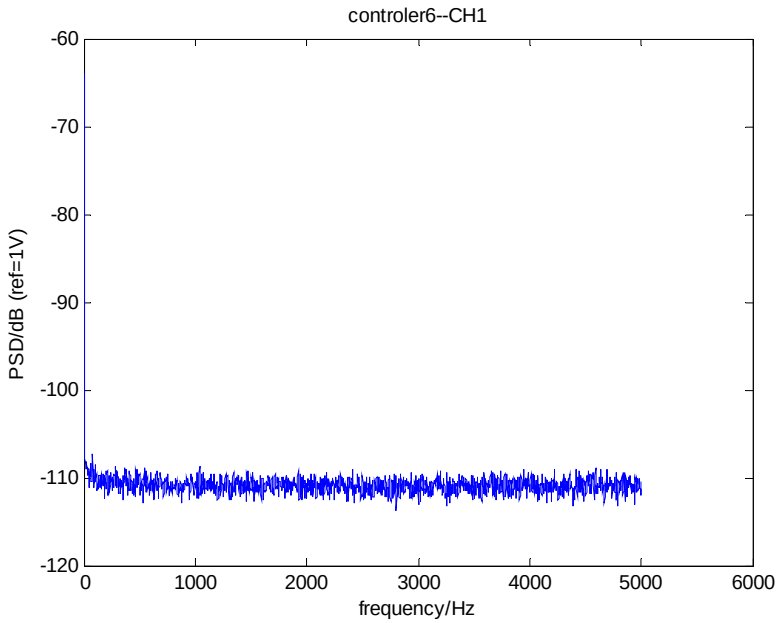

Figure 10: The crosstalk of input channel

6. Conclusions

This paper presents a design of and implementation based on TI's 66AK2H14 DSP to enable a highly efficient active noise and vibration control system. The results have reported that the proposed platform can well meet the required processing speed and accuracy for most applications.

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