Institute of Acoustics

A MICROPROCESSOR-BASED CODEC FOR A LOW-COST DIGITAL TAPE RECORDER

T. Donnelly (1), D.J. Mapps (1) and R. Wilson (2)

(1) Plymouth Polytechnic, Devon.
(2) Leeds Polytechnic, Yorks.

1. INTRODUCTION

The widespread application of digital techniques has generated a complimentary demand for cost-effective digital-data recording systems.

Personal computers (PC) are capable of generating vast amounts of data at reasonable cost. These data are usually stored on hard or floppy disc backed up by tape storage systems. In the entertainment field the storage and handling of music in digital form is commonplace. Digital tape systems have been employed at the professional level for some time and in the consumer field the compact disc (CD) is now being followed by the rotary-head, digital-audio tape recorder (R-DAT).

A further area where digital recording techniques are employed is that of data logging. Here, convenience and equipment portability are seen as attractions in addition to low cost.

The virtues of convenience, low-cost and portability are exemplified in the compact-cassette tape system. Although originally designed for analogue recording it may be adapted to record digital data directly. The computing power of a PC may be utilised to perform the function of a CODEC thus removing the requirement for much of the coventional circuitry normally associated with a digital recording system. Through the use of a PC and the adoption of a multitrack format a moderately high-density tape storage system may be realised at a low cost.

This paper reviews the techniques employed to realise a microprocessor-based CODEC by presenting two digital tape recorder systems: a basic recording system and an enhanced system. However, before detailing these techniques two major problems associated with the low-cost format of compact cassette will be considered: tape-velocity variation and tape skew.

Since information to be recorded is encoded in terms of the distance between magnetic flux changes the velocity of the tape must be constant. Low-cost tape decks, such as those used with compact-cassette tapes, suffer from velocity variation. To combat this, speed-control circuitry is often employed. Even so, speed related errors can occur if this problem is not fully accounted for.

A more serious problem is tape-skew variation (fig.1). As the tape moves across the headstack the skew angle varies about zero. Previous work on the measurement of skew [1] has shown that the rate of change of skew angle is of the order of 2 Hz and its magnitude is sufficient to give a displacement across the tape normally occupied by one bit at a recording rate of 10kb/s. The effect of tape skew on a single track is to reduce the effective read gap of the replay head and so reduce the amplitude of the detected signal. The effect on multitrack recordings is that data recorded broadside across the tape may not be sensed in the order in which they were recorded thus causing errors.

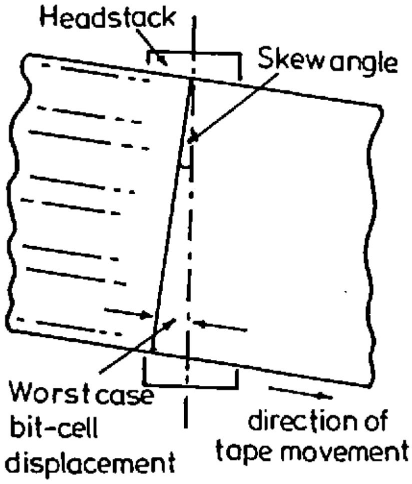

Fig.1 Tape passing headstack with skewed motion.

2. BASIC RECORDING SYSTEM

A basic recording system may be configured as shown in fig.2. The 4-track record/playback head is of the type normally found in auto-reverse audio tape recorders, an erase head is not required. Data are recorded by applying complimentary signals to each of the four head coils from the 8-bit peripheral input/output (PIO) chip of the PC.

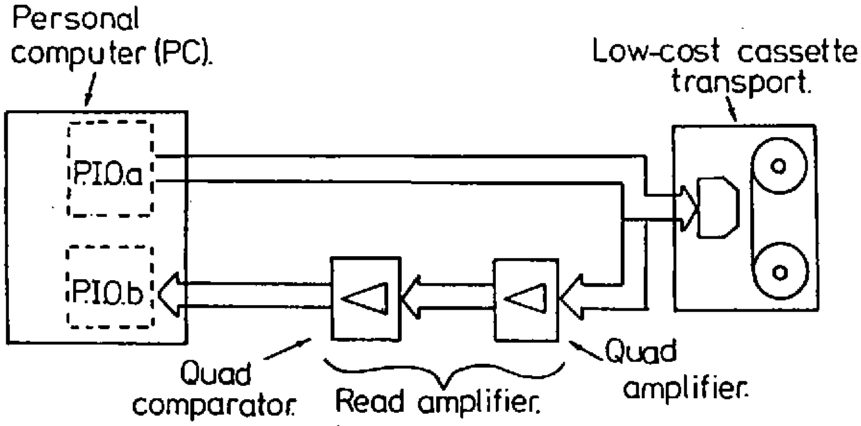

Fig. 2 Basic recording system.

A resistor should be placed in series with each coil to set the record current to approximately 2 mA. The read amplifier is the only conventional hardware required. It amplifies and slices the low level tape signal before application to a second PIO.

Software is used to encode, detect and decode data. A recording code which has been used with some success is Biø-L code (fig.3). To record, the compliment of the data are transmitted followed by the true value. The data may be timed by using a software timer or the internal counter/timer of the PC may be utilised. The parallel bit structure of the PC permits each track of the tape to be simultaneously recorded, one bit of the processor word per track.

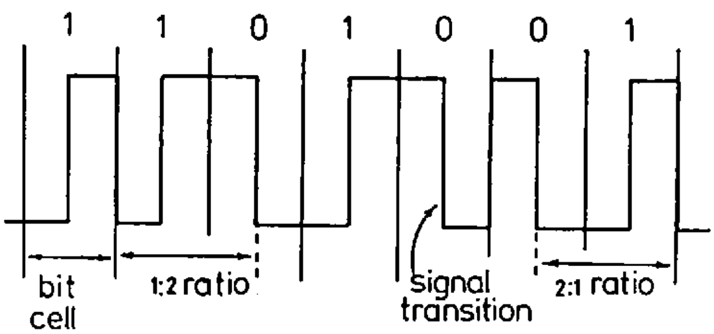

Fig.3 Biø-L code.

Biø-L code has a number of features which make it suitable for software implementation in this application. With Biø-L code a change in signal level always occurs at the centre of the space occupied by one bit - the bit cell. Also, the ratio of intervals between three successive transitions of the signal can be used to identify either the bit-cell boundary or the bit-cell centre. A 1:2 ratio of two successive intervals marks the bit-cell centre whereas following a 2:1 ratio the bit-cell boundary is reached. This characteristic is used in the decoding process.

The decoding software polls the output of a single track and times the interval between transitions. The ratio of successive intervals is computed and the result indicates the current point within the bit cell. If a 1:1 ratio is encountered it is ignored. Because ratios are involved this method of synchronising to the data is tape-velocity independent.

The process of measuring and computing the ratios is continuous. Each time a 2:1 or a 1:2 ratio is measured the "1" value is stored in the PC and is used by the software to calculate an accurate sample point which is halfway through the second half of the bit cell. This method of determining the sample point is also independent of tape velocity.

Although the sample point is determined by synchronising to a single track all four tracks are simultaneously sampled at this point. The attraction of this technique is the simplicity of the software required. However, skew-generated errors will occur especially at the higher data rates.

A software refinement of the technique is to make the track to which the software synchronises variable. The advantage of this is that the first track signal to change in time (the leading track) may be used for synchronisation and the sample point determined as late as possible within this bit cell. Since the three other track signals will change some time after the leading track signal (due to tape skew) the late sample point will coincide with the three track signals in the second half of their respective bit cells and, if the total skew is within ± 1/2 bit cell, the data will be sampled without error. This technique effectively doubles the tape- skew tolerance of the software compared to the simple arrangement described above.

Results showing error rate against data rate are shown in fig.4. The advantage of synchronising to the leading track is clearly seen. The execution time of the software limited the data rate to 2.5 kb/s/track. However, the software included error-verification procedures and the clock rate of the microprocessor used was only 4 MHz. This data rate is capable of being significantly increased by the application of a faster processor and the elimination of the error-verification software overheads.

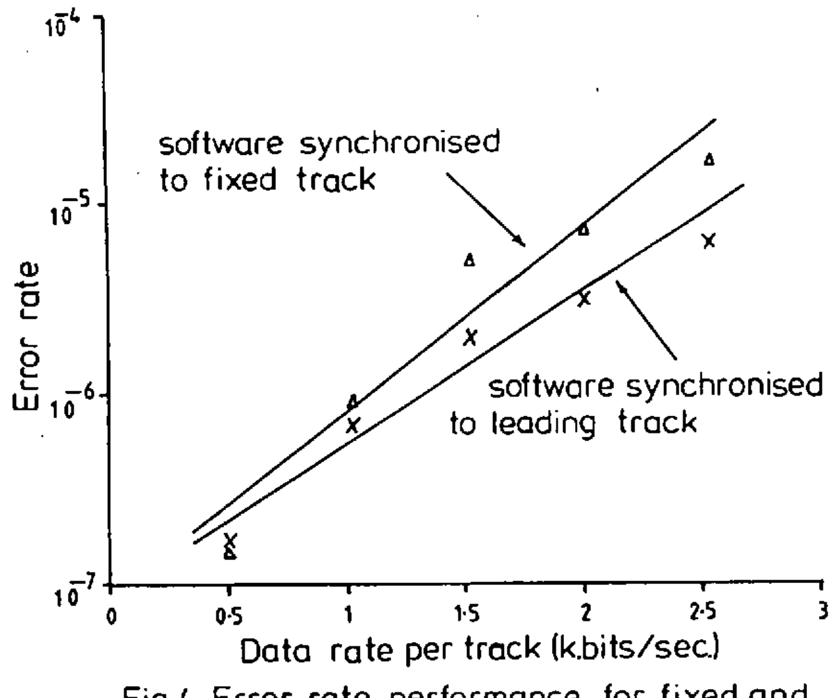

Fig 4. Error rate performance for fixed and variable synchronisation.

3. ENHANCED RECORDING SYSTEM

With the addition of specialised de-skew and clock hardware the performance of the basic system of fig.2 may be improved. In this enhanced recording system an 8-track head is used and the recently developed ISS 2/3 [2] recording code is employed to give a recording rate of 10 kb/s/track. With the ISS 2/3 code two data bits are recorded as three code bits (Table 1). The advantage of this code is that since no adjacent ones are allowed to occur a greater recording density can be achieved. A code sequence which would give two adjacent ones is deemed illegal and is replaced by a code sequence conforming to the rules of the code (Table 2). Although originally developed for recording data serially a parallel software algorithm for the ISS 2/3 code has been devised for this application [3].

The two outside tracks of the tape are encoded with control pulses whilst the six inner tracks are occupied by data. The control pulses serve two functions. They are spaced every three code bits so that the decoding software can identify each code-bit group. The de-skew hardware also uses these control pulses to calculate the tape skew.

Data	Code
00	101
01	100
10	001
11	010

Table1. ISS 2/3 Encoding table.

Data	Illegal code	Replacement code
0000	101101	101000
0001	101100	100000
1000	001101	001000
1001	001100	010000

Table 2. Illegal code sequences and their replacement.

In this system a hardware clock is used for each of the six inner tracks. On replay these clock the code bits off each track into one of two data flip-flops associated with each of the six data tracks (fig.5). The pulses on the two outer tracks are used to measure the magnitude and polarity of the prevailing tape skew. The output of the skew measurement circuit comprises six pulses each of which is used to control the clock input to the data flip-flops. The time over which the sequence of six pulses occurs is equal to the time displacement across the tape due to skew. Thus, the six data bits, which were recorded across the tape, are routed into their respective data flip-flop after which they are multiplexed into the microprocessor. Two sets of registers are used to give an acceptable tolerance to tape skew at this recording rate. This may be increased by employing more than two sets of registers on a proportional basis.

The error rate of this system was assessed by recording a "sawtooth" waveform digitised to six bits resolution. On replay the waveform was decoded and outputted to a digital-to-analogue (DAC) convertor where it was viewed with an oscilloscope. Although performance was marred somewhat by an excessive amount of inter-gap crosstalk within the replay head the sawtooth remained in "synch" failing only when the skew measurement circuit was disabled.

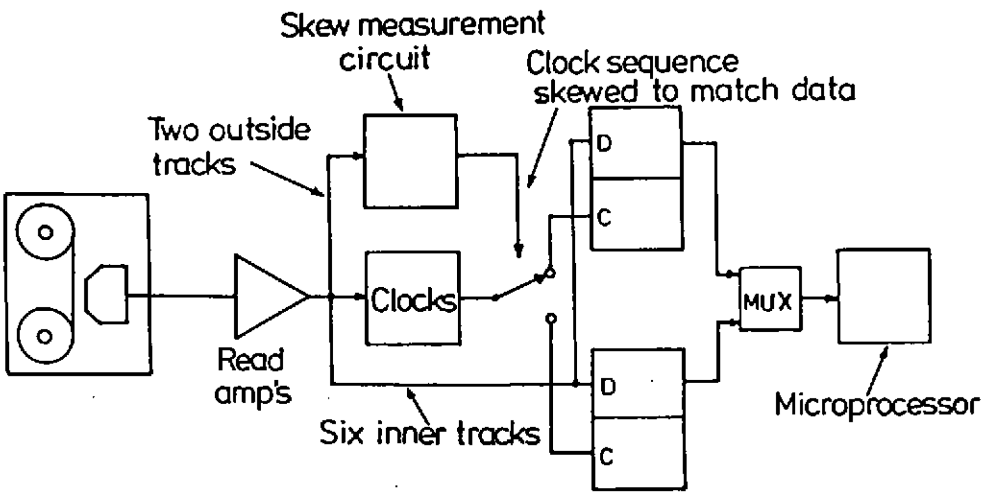

Fig.5 Enhanced recording system.

4. CONCLUSIONS

A microprocessor-based CODEC has been implemented to produce a low-cost digital tape recorder. Two, direct digital compact cassette recording systems are presented. Data are recorded on proprietary audio compact-cassette tapes.

With the basic system a data rate of 10 kb/s has been achieved with a reasonable error count. This could be significantly increased with the application of a faster processor. An 8-track head may also be used with the same software to double the data rate. The system may be applied as a low-cost data logger, it could also be used to store low-grade digitised audio signals where data compression techniques are employed.

The second system gives an improved performance but specialised hardware is required and the 8-track head used is not a standard item. Once again a faster processor could be applied either to increase the data rate and/or reduce the specialised hardware requirement. A further improvement would be to integrate data and control pulses on the outer tracks and thus improve the data rate by 30%.

Currently under development is the application of an 18-track, thin-film magneto-resistive head which will be used with the software developed for the above systems run on a 16-bit microprocessor.

5. REFERENCES

[1] Donnelly, T., Mapps, D.J., and Wilson, R. 'Real-time microprocessor monitoring of skew angle in a compact cassette multitrack magnetic tape system'. J. Inst. Electronic & Radio Engineers. 56, No.2, pp.49-52, February 1986.

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[3] Donnelly, T., Mapps, D.J., and Wilson, R. 'High density data storage on audio compact cassette tape using a low-cost tape transport'. J. Inst. Electronic & Radio Engineers, 57, No.5, pp.232-238, Sept/Oct. 1987.