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HIGH PERFORMANCE SIGNAL ACQUISITION SYSTEMS FOR SONAR APPLICATIONS

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1. INTRODUCTION

Very large scale integration (VLSI) produces digital signal processing (DSP) systems with massive computing power at a modest cost. However, the overall performance of such systems in real time sonar applications is often limited by the front end signal acquisition circuits feeding the digital processors, where cost, power and volume constraints force the system designer to make a number of practical engineering compromises. These arise when mapping a conceptual front-end design (i.e. linear, wide dynamic range) onto standard, commercially available components initially developed for other signal capture applications, often with very different system parameters and design aims.

This implementation/performance trade-off can be by-passed in critical DSP areas [1], using computer aided design (CAD) tools to generate VLSI application specific integrated circuits (ASICs), in high density gate array or macro-cell technologies. However, the VLSI ASIC technologies do not produce good analogue circuits: indeed, the very improvements in semi-conductor device geometries that allow the high level of integration needed for DSP result in devices with degraded analogue signal handing capabilities and, although emerging mixed analogue/digital technologies like BiCMOS go some way towards redressing the balance, current silicon ASIC technologies provide only limited dynamic ranges (around 80 dB) in front-end circuits where a significant amount of analogue circuitry is integrated with complex digital logic. Consequently the cost/performance ratio and the lack of integrated analogue CAD tools do not yet make mixed analogue/digital ASIC front end designs cost effective in sonar applications: this situation will change as the mixed technologies mature.

Full custom device development, in either low voltage CMOS or BiCMOS, is possible for front end circuits but the high development cost and low volume requirements in sonar do not make this attractive either, except in a few very high value-added applications.

Consequently, most sonar front-end designs use devices and techniques developed in the first instance for other high volume applications, for example for digital audio or telecommunications systems. This limits the choices open to the system designer and, as well as potentially limiting operational sonar performance, constrains data acquisition system

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architectures, particularly in large aperture systems with large numbers of sensors: it also generates more complex system designs than may in fact be necessary in the critical analogue areas before digitization.

2. SOME PROBLEM AREAS

Figure 1 shows a schematic of a typical conventional data acquisition system using "off-the-shelf" components: analogue transducer signals are amplified and fed via anti-aliasing filters and multiplexers to analogue-to-digital converters (ADCs); digital data is then further multiplexed and transmitted to the signal processing system.

This form of signal acquisition system architecture, utilising a combination of analogue and digital multiplexing, results from the need to maximise the number of channels handled by each ADC, in order to minimise sub-system cost and power dissipation. Successive approximation ADCs, with resolutions ranging from 8- to 16-bits, (the latter developed mainly for commercial DAT and CD applications), are readily available from commercial sources: the relatively fast conversion time of these components, typically less than five microseconds, provides ADC-channel sample rates in excess of two hundred kilohertz, much higher than that required for individual hydrophone channels in large aperture array applications. Consequently, a number of channels are multiplexed through each ADC, with each channel sampled at a few times the Nyquist rate, in order to use this conversion bandwidth effectively.

The potential dynamic range for a 16-bit ADC is around 96 dB [2] but the considerable amount of analogue circuitry required around the ADC to use its throughput efficiently and the need to ensure that a sufficient number of bits are toggling when minimum signal levels are being received, for proper operation of the following digital processes, reduces this figure somewhat in practice.

One particular problem area is the design of the anti-alias filters to band limit the hydrophone signals before sampling. To maintain a 96 dB signal-to-noise (or signal-to-image artifact) ratio, the filter out-of-band rejection must be of the same order: the filter must also provide low in-band ripple and sharp transition bands and, in multi-channel systems, gain and phase matching between channels must be maintained to close tolerance. Taken together, these requirements dictate the use of high order filter designs, (typically ninth order elliptic low pass), and these are difficult to produce using available monolithic filter technology. Switch capacitor filter techniques [3] do not provide sufficient dynamic range, whilst channel matching is a problem in continuous time (differential-integrator) filter implementations [4]. Functionally adjusted laser-trimmed thick film hybrid technology [5] will provide the level of performance needed, but even here channel-to-channel matching can be a problem.

Similar design problems occur in the other pre-digitization circuits due, for example, to charge feed-through on the semiconductor switches used for the analogue multiplexing and in the sample-and-hold circuits and even the relatively straight-forward parts of the system are pushing the limits of IC technology. Consider, for example, the hydrophone pre-amplifiers: these receive and amplify low level signals from the transducers, typically a piezo-electric hydrophone element with a source capacitance of, say, a few hundred picofarads. In many applications, frequency cover down to a few hertz is necessary and transducer sensitivities/acoustic source levels are such that hydrophone signal voltage levels of 5-10 nV/√Hz at 10 Hz are typical. Interfacing voltages this low, from a high impedance capacitive source at low frequency, is difficult if conventional operational amplifier circuits are used: operational amplifiers with sufficiently low voltage and current noise at low frequencies are available [6], but the power required for a single operational amplifier with the necessary performance is high, typically in excess of 100 mW, and this causes problems when developing large, power sensitive systems. Low power dissipation, high performance sonar pre-amplifier circuits still require discrete JFET/bipolar designs.

As a result of the problems outlined above, the system shown in Figure 1 may provide signal-to-noise ratios of only around 60-80 dB in practice, unless great care is taken with component selection.

The signal dynamic range that the system can handle is in fact much less than this: array data is usually beamformed immediately after digitization and this process requires data with sufficient resolution. Vural [7] has shown that at least four-bit resolution data is needed for beamforming to avoid losses in array gain. Vural's analysis was for the classical case of a point target in spatially homogeneous white noise. When more realistic structured targets in non-homogeneous, non-white noise and reverberation are considered, the number of bits required for efficient beamforming increases: current systems would normally allow a minimum of 6- to 8-bits toggling. This need to maintain a minimum digital signal level reduces the effective instantaneous signal dynamic range of a circuit like that in Figure 1 to around 30 dB, and this is not sufficient in many scenarios when large temporal, spatial or spectral fluctuations in acoustic level are experienced.

Wide signal dynamic ranges appear on arrays that operate in areas where the ambient background is normally quiet but where high level acoustic transients occur or noisy interfering sources need to be countered. Such conditions are found, for example, when geophysical or oil industry related activities are being carried out nearby (i.e. in the same ocean basin), when both active and passive signals are received at the same time on the same array, or when operating in acoustic environments corrupted by local noise sources, etc. Converter dynamic ranges up to 120 dB are needed to maintain adequate system performance under these conditions. High linearity acquisition systems are also important when developing arrays for adaptive processing.

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3. POTENTIAL SOLUTIONS.

In the past, various techniques have been used to minimise the complexity of both the conversion system itself and of the digital processing that followed but the resulting hardware simplifications were usually obtained at the expense of overall system performance.

Digital techniques were first applied to sonar systems in the 1950s [8] and early systems, such as DIMUS [9] used hard clipped hydrophone data and simple single bit processing systems. Clipping degraded the system performance, due to clipper quantisation and capture effects [10] and multi-level systems with low resolution ADCs were developed in the mid/late 60's. These gave some improvement in performance but various capture effects were still apparent due to the use of gain control circuits before conversion: the limited dynamic range available with early converters necessitated automatic or time varying gain control circuits to minimise received signal level variation and to keep it within the input range of the converters. The resulting gain variation effectively modulates the received signals with a time varying function and this modulation process generates time and frequency smearing of the signals and a corresponding reduction in system processing gain. In active systems, modulation gives rise to decorrelation and multiple target ghosting, whilst in narrow-band passive systems it introduces tonal smearing and reduces lofargram detectability.

The rapid progress in ADC technology during the 1970s and '80s produced higher resolution converters, with 12- and 16-bit parts soon becoming available. However, these were, in the main, designed for particular high volume applications and not ideally suited to use in sonar systems due to the problems outlined in Section 1 above.

The ideal parameters for a high performance data acquisition system for large aperture sonar are subtly different than for telecommunication or digital audio applications:

1. transducer arrays are multi-channel sensors, rather than the one or two signal channels processed in most other applications,

2. sonar bandwidths are low, usually only a few kilohertz,

3. signal dynamic range can be high, typically up to 120 dB

4. channel-to-channel gain and phase matching must be good,

5. power dissipation needs to be minimised, particularly in remotely deployed or towed arrays, (ideally less than 10 or 20 milliwatts per channel in large towed systems to avoid power distribution problems, less still in remotely deployed applications),

and 6. size and cost are critical due to mechanical limitations and the number of channels (maybe several thousand) in large aperture systems.

The technology choices available to the sonar designer are limited if highly integrated sub-system designs to meet the general specifications listed above are considered. From the previous discussions, fully monolithic acquisition systems are not yet feasible: any development would need to exercise a mix of technologies to achieve the required performance level and given that at least part of the data acquisition system (the pre-amplifiers) will need to be discrete, then either surface mount [11] or thick film hybrid technology appears to provide a reasonable vehicle for data acquisition system integration. Both technologies have the advantages of already being widely used in military systems and of low tooling and production costs. (They are also both available in house at ARE, Portland.)

Production thick film components can be matched to within 0.1% easily, using functional test and laser trim, and to within 0.05% with care. These tolerances are significantly better than those that are readily available with monolithic silicon technologies and the excellent component matching with laser trim thick film can be exploited in high performance circuits. Whilst the technology could be used to produce a hybrid successive approximation ADC, the circuit complexity needed is prohibitive and it would be difficult, even with 0.05% component matching, to achieve much better than 16-bit resolution on a production basis. However, the signal channel bandwidths required for sonar are much less than for most other applications and techniques that exploit the intrinsic component matching in the analogue area of the circuit and extend the dynamic range of a lower resolution converter by over-sampling and interpolation are possible avenues to improved converter performance.

Ideally one would like to reduce and simplify the analogue content of the signal acquisition systems as far as is possible: one possible way to achieve this is to trade some of the analogue circuit complexity for an increase in the digital signal processing load, as the latter can be provided economically using custom ASIC designs. The balance resulting from this trade allows analogue technology mixes to be considered that provide improved performance at lower cost and power.

Consequently a number of ADC techniques [12] that could be used in low analogue complexity, oversampling converter architectures were reviewed and, in some cases, bread-boarded: the results of this review are given below:

1. Flash converters: very fast - conversion time = 1/(sample rate). High analogue complexity, one analogue stage for every level. Impractical for high accuracy, typically resolution limited to less than 10 bits. Requires considerable amount of digital logic to encode comparator outputs. Complexity can be reduced by sub-ranging, but this also increases conversion time.
2. Pipeline converters: very fast - conversion time approx.

1/(sample rate), but converter latency due to the pipeline. Moderate analogue complexity, typically one analogue stage per bit. Moderate accuracy possible, resolution typically up to 14 bits.

3. Successive approximation converters: moderate speed, conversion time = (no. of bits)/(sample rate). Few analogue stages used, but ladder matching important. Medium accuracy, typical resolution 14-16 bits. Moderately complex digital circuitry.

4. Dual slope (integrating) converters: extremely slow, conversion time = (no. of levels)/(sample rate). Very simple analogue circuitry. Extremely high accuracy possible, resolutions in excess of 20 bits possible. Moderately complex digital circuitry.

5. Oversampling noise shaping (sigma-delta): moderately slow, conversion time = (oversampling ratio)/(sample rate). Simple analogue circuitry. Extremely high accuracy possible, resolutions in excess of 20 bits possible. Very complex digital circuitry required for decimation filter. No sample-and-hold or anti-aliasing filter required at input.

Of the techniques listed, only those with low analogue complexity that mapped easily onto surface mount or thick film hybrid technologies were considered for further development, and at first sight, both the dual slope and the sigma-delta converter are attractive. However, the high operating clock rate required for high resolution conversion, even for low converter bandwidths, limits the utility of the dual slope technique: for example, 20 bit resolution with, say, 500 Hz signal bandwidth requires clock rates in excess of 200 MHz, not practical in power sensitive applications.

Consequently the most promising technique is sigma-delta: this has the added attraction that converter circuits can be designed without the need for complicated sample-and-hold circuits and anti-aliasing filters, (the initial data sampling rates at the front of the converter are high and band definition is provided by the following digital processing): this removes two of the limiting analogue areas in "conventional" signal acquisition circuits. These advantages are however achieved at the expense of an extremely complex, high performance digital decimation filter and this requires a custom ASIC DSP design for a compact, low power implementation.

4. FROM SINGLE BIT CLIPPER TO MULTI-BIT CONVERTER.

A large number of papers on sigma-delta converters [13] have appeared in the open literature over the past few years; most discuss converters implementation, usually in full custom silicon, and demonstrate the level of

performance achieved. Few attempt to quantify the potential performance limits and the possible technology/architecture trade-offs available with the technique in any formal way. (One major problem in this area is that the theoretical understanding of non-linear systems for signal processing does not appear to have progressed much beyond the classical work of Bennett and Rice [14] and Davenport and Root [15]. This area appears to be another where a small amount of theoretical research could pay good dividends in terms of practical circuit payoff).

The following paragraphs take a similar route and outline a simple derivation of the multi-loop noise cancelling sigma-delta converter: no attempt is made to compare the many sigma-delta converter architectures that are possible, and the circuit topology described was chosen simply to exploit the component matching in hybrid thick film and surface mount implementations.

4.1 The Hard Clipper.
The clipper can be considered as a one-bit flash ADC: when a time domain signal feeds to the clipper, its output voltage can be considered as a linear combination of the input signal plus some error signal or quantisation noise, i.e.:-

$$V_{out}(t) = V_{in}(t) + V_q(t)$$

The clipper output spectrum can be calculated, using the characteristic function transform method [15], for simple input signals such as narrow band CW signals where the clipper output flips state at the zero crossings of the input signal and generates a square wave output. With more realistic input signals, the output spectrum becomes more complicated; for example, for two sinusoids at different frequencies at the input, the spectrum contains a collection of inter-modulation as well as harmonic terms.

Since the clipper output level will sit at either $+V_{out}$ or $-V_{out}$ for all input signal levels, the output energy (and power) will be constant, independent of the input signal level and, whilst the total output energy must remain constant, it may be able to shape the quantisation noise spectral density so that it lies mainly outside the required signal frequency band.

4.2 Linearising the Clipper.
Varying the amplitude of a signal at the clipper input will not affect the output waveform of the clipper, so the spectral density of clipped signals is not proportional to their input levels. It would be convenient to find some way to modify the clipper transfer function, so that output and input levels are linearly related and cross product and harmonic terms minimised. Davenport and Root show that if the clipper input is a narrow band signal in gaussian noise, then the output signal/noise ratio becomes asymptotically equal to the input signal/noise ratio as the input signal/noise ratio is reduced. This is effectively linearising the transfer function of the clipper, as far as the signal is concerned, so one possible way to improve linearity is to add a random dither to signals before clipping.

Unfortunately, it is not possible to remove this dither signal after clipping as this would require a detailed knowledge of the signal itself to calculate signal/dither interactions in the non-linear clipping process. However, if a deterministic dither, related to the clipper input, is used then it is possible to cancel the its effect after clipping.

Consider, for example, generating a voltage equal to the quantisation noise introduced by the clipper, by differencing the clipper input and output signals, and using this as the randomizing dither signal as shown in Figure 2(a). This circuit can be re-drawn as shown in Figure 2(c), a first order sigma-delta converter with the transfer function:-

$$V_{out}(t) = V_{in}(t) + V_q(t).\ (1 - z^{-1})$$

The clipper quantisation noise, $V_q(t)$, is suppressed by the $(1 - z^{-1})$ term in the transfer function: in a practical system, the z^{-1} delay may be generated by some clocked circuit, strobed by the sampling clock at a frequency F_c and, if the signal frequency F_s is much less than F_c, then the noise reduction due to the $(1 - z^{-1})$ term is significant. The variation of this term with the oversampling ratio $(=F_c/F_s)$ is shown in Figure 3: the suppression term rolls-off at LF at approximately 6 dB/oct, with around 25 dB noise suppression for 100 times oversampling.

4.3 The Multi-loop Sigma-delta Converter.
The noise suppression obtained using the clipper within a high gain feedback loop is useful, but very high oversampling ratios are required to use this technique directly in high resolution systems: it can also be shown that the quantisation noise spectrum in a single sigma-delta loop is correlated with the input signal and that its spectrum is discrete and highly coloured [16]. Further suppression is required for practical applications: this can be obtained by feeding the clipper error term to further sigma-delta loops, for example the third order system (three loops) shown in Figure 4. The transfer function for this circuit is of the form:-

$$V_{out}(t) = V_{in}(t) + V_{q3}(t)\ .\ (1 - z^{-1})^3$$

where $V_{q3}(t)$ is the quantisation noise due to the clipper in loop 3.

The quantisation noise from the each loop in Figure 4 is effectively cancelled (in the combining circuit) by the output from the following loop. This however generates its own noise, but this is modified by the noise shaping term $(1-z^{-1})^N$, where N= 1,2,3 - the loop number. The variation of these noise shaping terms with oversampling ratio, normalised for constant total energy, is plotted in Figure 5. The three loop converter has a low frequency quantisation noise suppression term roll-off of 18 dB/octave, around large suppression for a signal with an oversampling ratios in excess of 100.

The quantisation noise suppression is easy to calculate but the noise spectrum for the multi-loop converter is more difficult to quantify. It can be shown [16] that the quantisation noise from the third loop (i.e. V_{q3}) is uncorrelated with the converter input signal and that its spectrum is flat. Computer simulation indicated that the quantisation noise, harmonic and cross-product levels for a practical hybrid three-loop circuit, with an oversampling ratio of 128, will provide signal/noise (or signal/artifact) ratios in excess of 120 dB.

Further reductions in quantisation noise can be realised by replacing the hard clippers in the sigma-delta loops by multi-bit flash converters. This then requires a multi-bit digital-to-analogue converter (DAC) to feed signals back to the loop integrators: simple analysis shows that these will determine the overall circuit linearity and that DAC linearity must be of the same order as the required converter resolution i.e. in excess of 20-bits: one bit DACs are intrinsically linear, two-bit DACs can be made so with some simple circuit tricks, but higher DAC resolutions require the use of fairly heavy linearising techniques [17].

The sigma-delta loops are sampled time, analogue circuits. They produce three separate digital outputs that are combined to generate a heavily over-sampled, multi-bit data stream: this is filtered and decimated to generate the high resolution ADC output.

5. DIGITAL PROCESSING - DECIMATION FILTERING.

The over-sampled, multi-bit combiner output has to be low-pass filtered and decimated to reduce the quantisation noise and to generate the high resolution signal data. The performance of this filter is critical to the operation of ADC: it needs to have an out-of-band attenuation of the same order as the required resolution (in this case >120 dB), low in-band ripple and a sharp transition band.

Most published sigma-delta implementations are aimed at 16-bit resolution and use a combination of notch and decimated FIR filters [18]. FIR architectures require considerable processing power when implementing high performance filters: for high precision systems, recursive multi-rate wave digital filter (WDF) structures [19] prove more efficient. The WDF has the advantage of requiring around only one fifth of the processing power of a decimated FIR with similar performance [20]. The basic WDF section is shown in Figure 6(a); each section decimates by a factor of two, and hence seven cascaded stages are required for an over-sampling ratio of 128. Figure 6(a) shows a schematic for each filter section and the overall frequency response of the filter is plotted in Figure 7: note that only around two multiplications per input data sample are needed to achieve this performance.

6. PRACTICAL IMPLEMENTATIONS.

The three-loop sigma-delta converter shown in Figure 4 needs some modification for easy implementation in hybrid technology. In particular, the sampled-time integrator can be more conveniently realised as a continuous-time RC-integrator in thick film. The three-loop system is re-drawn as a practical schematic in Figure 8: discrete component matching in this circuit is critical, as loop response matching determines the degree of quantisation noise suppression achieved in practice: signal/noise ratios in excess of 140 dB have been measured with laser trimmed thick-film substrates. The degree of matching available in thick film is not obtained in any of the monolithic silicon technologies: other sigma-delta architectures [21] are needed to achieve high resolution on silicon.

An schematic of a practical ADC sub-system is shown in Figure 9: local voltage regulators, the hydrophone pre-amplifier, a low order anti-alias filter and circuits to serialise the converter output and to multiplex it onto a common highway, shared by from a large number of individual ADCs, via a time slot allocation circuit, are included to facilitate integrating complete data acquisition systems.

Realisations of this basic schematic, with various numbers of noise cancelling sigma-delta loops and with both one-bit and two-bit quantisation within the loops, have been built for a number of particular applications, using either thick film or surface mount technologies for the analogue processing and a custom VLSI ASIC for loop combination, filtering and data serialisation. Photographs of a complete converter are shown in Figure 10, with some typical measured output spectra in Figure 11. The main performance characteristics are outlined below:

Physical size	5cm x 1.8cm x 0.5 cm
Power requirements	+/- 5volts @ 3 mA
Output format	24 bit serial + parity
Input impedance	>30M//100pF
Converter harmonic distortion	-100 dB
Signal dynamic range	≈120 dB

SURFACE MOUNT CONVERTER PARAMETERS

7. DISCUSSIONS AND FUTURE PROSPECTS.

The previous sections demonstrate that complete, low cost, low power sonar signal acquisition systems with dynamic ranges in excess of 120 dB have been routinely produced using hybrid technology. The converter topology used exploits the passive component matching available in hybrids and whilst the analogue integrated circuits used are commercially available "jelly bean"

parts, the digital circuitry needs to be fabricated as a custom ASIC (around 30,000 gates complexity) if the converter is not to be prohibitively large. Testing these devices have proved something of a problem: signal sources with noise floors and harmonic levels commenserate to those realised with the converter itself. In consequence, special test gear was designed for most measurements.

Improved designs are currently under development to reduce the power consumption of the system by around an order of magnitude whilst increasing the converter signal bandwidth: these improvements are obtained using of an improved, lower slew-rate sigma-delta loop topology and lower complexity digital processing using a constrained coefficient WDF architecture (requiring only two hard wired binary shifts per section).

8. ACKNOWLEDGEMENTS.

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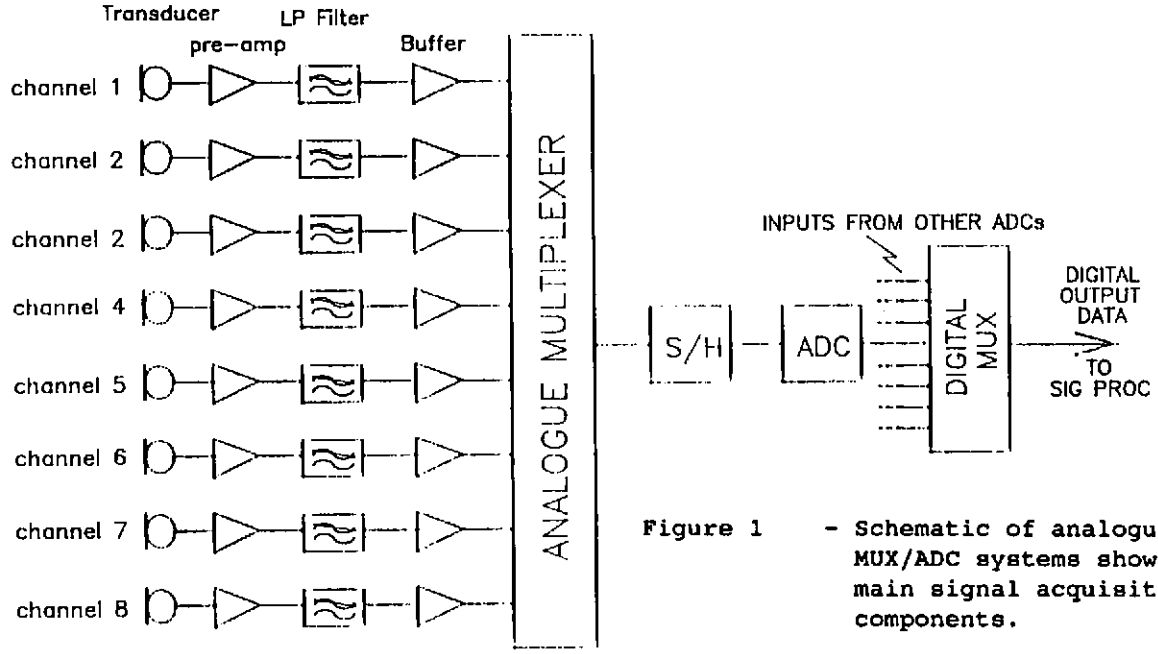

Figure 1 - Schematic of analogue MUX/ADC systems showing main signal acquisition components.

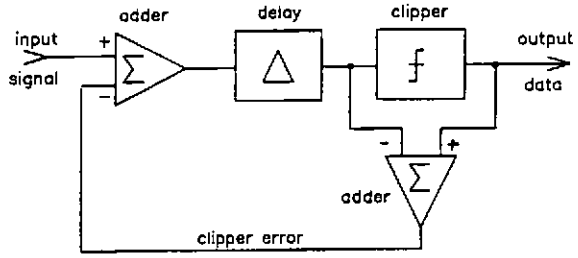

Figure 2(a) - Coherent dither schematic.

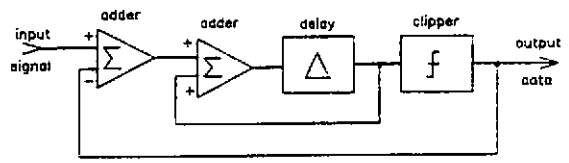

Figure 2(b) - 2(a) re-drawn to show integrator function.

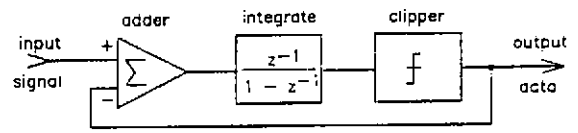

Figure 2(c) - First order sigma-delta converter.

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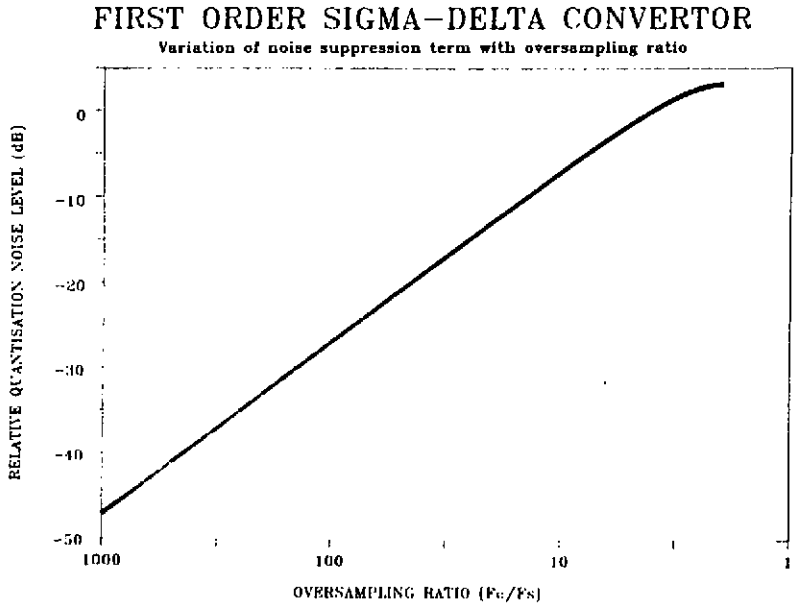

Figure 3 - Variation of noise suppression term with oversampling ratio.

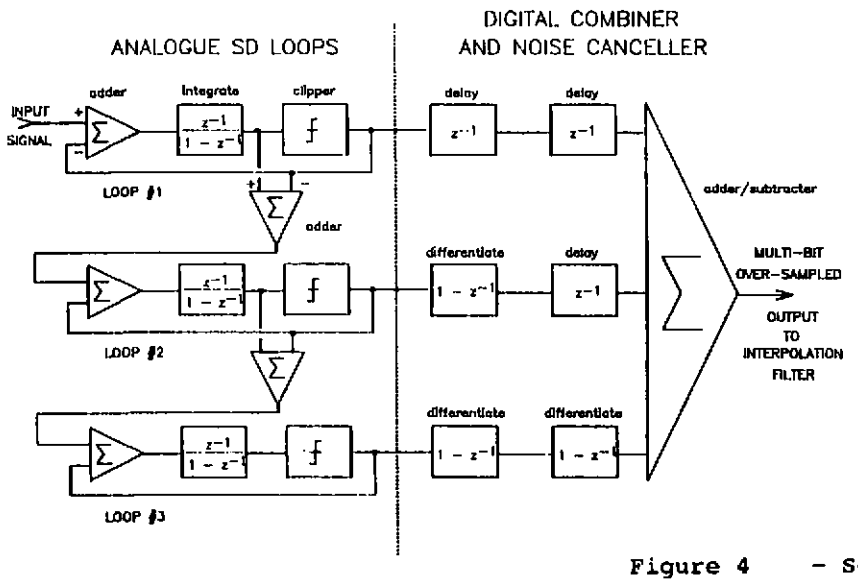

Figure 4 - Schematic of three loop, noise cancelling converter.

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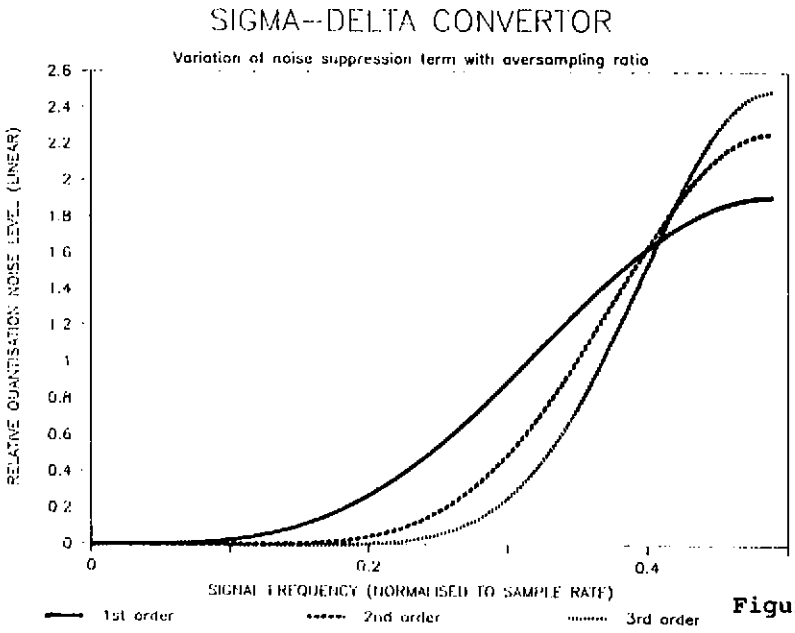

Figure 5(a) - Variation of noise suppression term with oversampling ratio - linear amplitude scale.

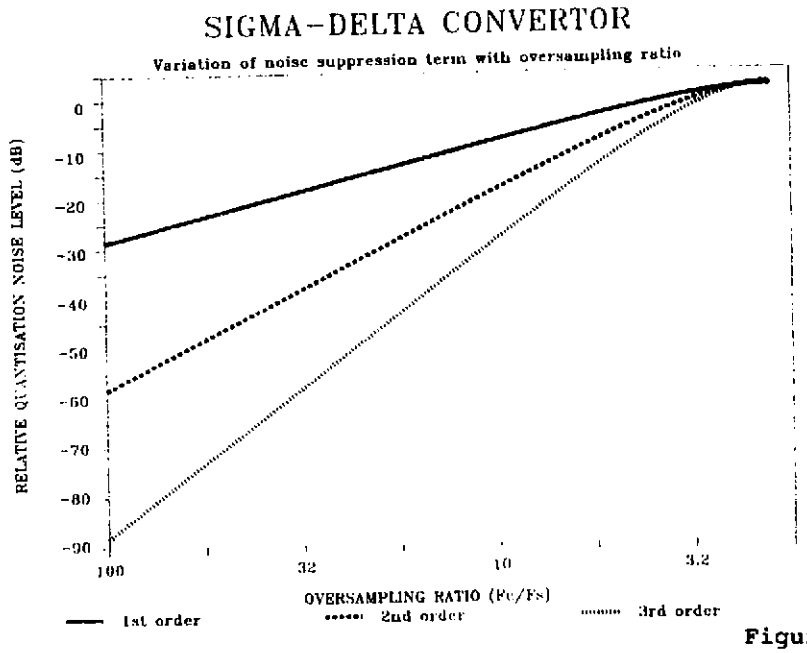

Figure 5(b) - Variation of noise suppression term with oversampling ratio - logarithmic amplitude scale.

HIGH PERFORMANCE SIGNAL ACQUISITION SYSTEMS FOR SONAR APPLICATIONS

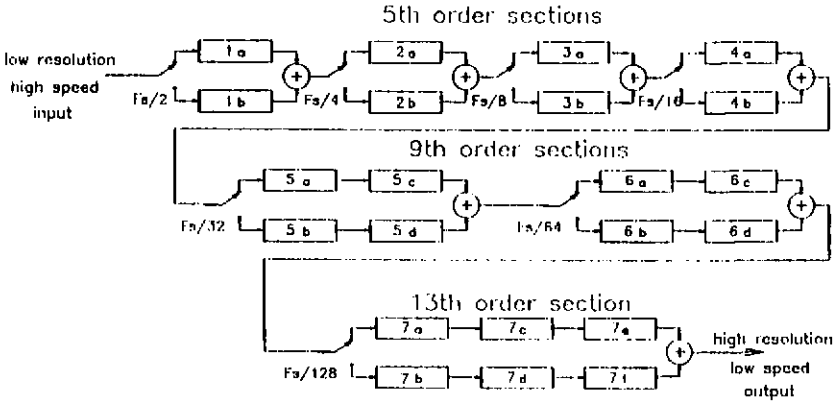

Figure 6(a) - Interpolation filter - overall structure.

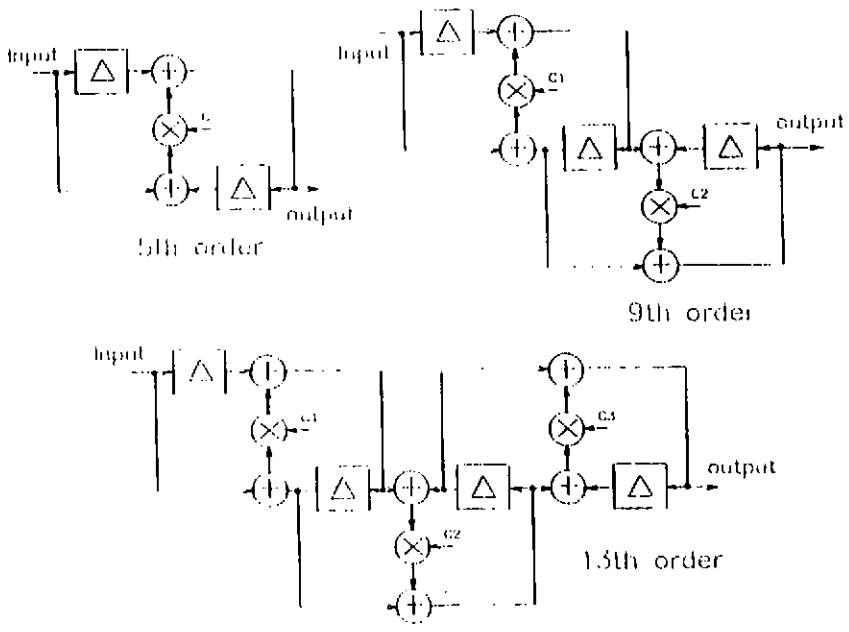

Figure 6(b) - Interpolation filter - section schematic.

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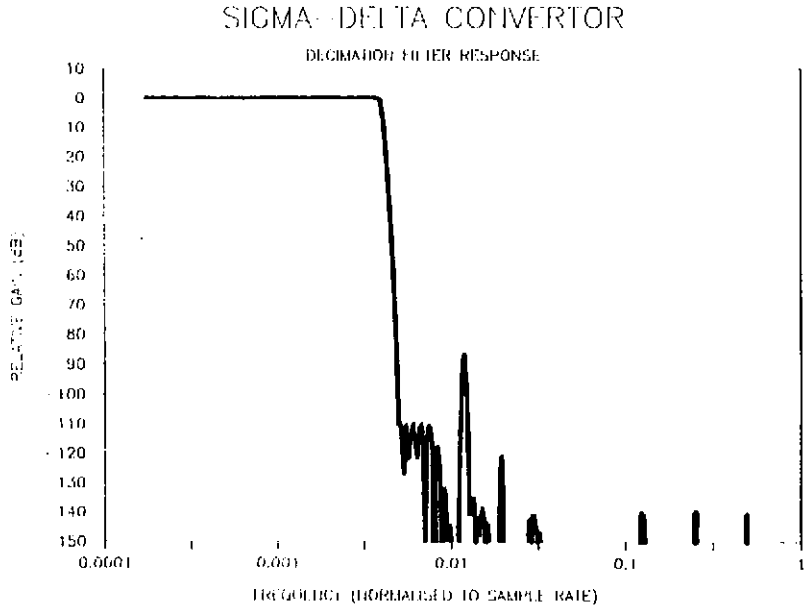

Figure 7 - Interpolation filter - overall frequency response.

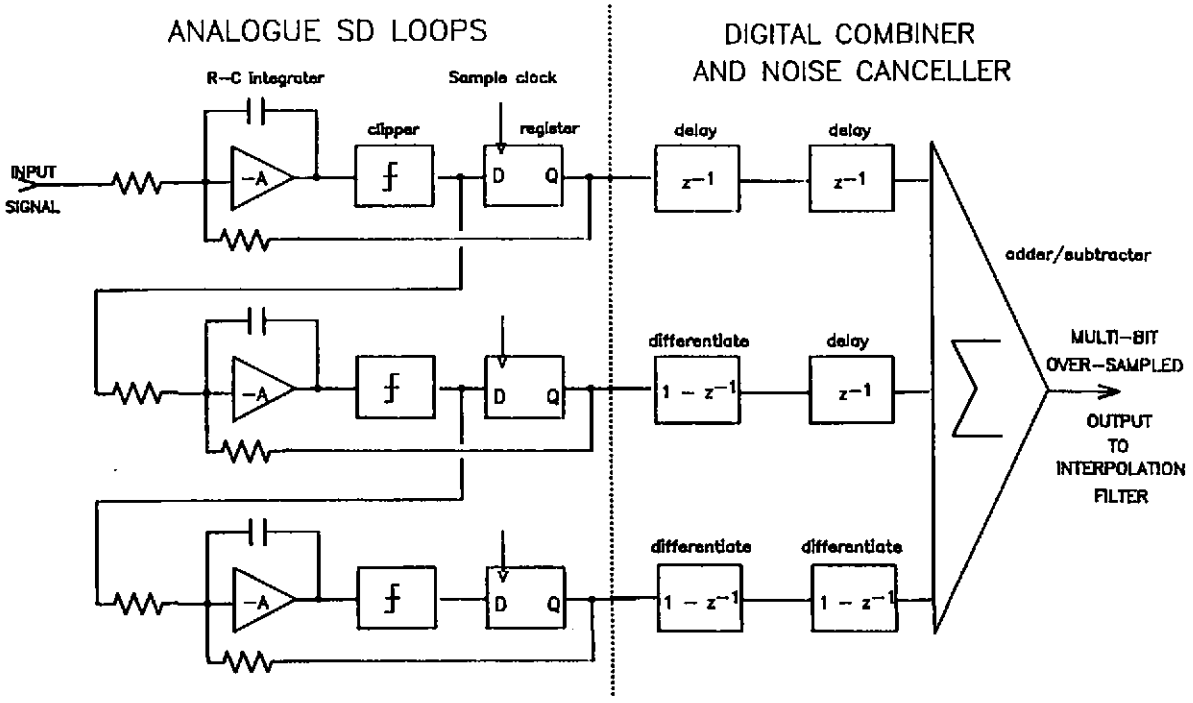

Figure 8 - Continuous time RC-integrator schematic.

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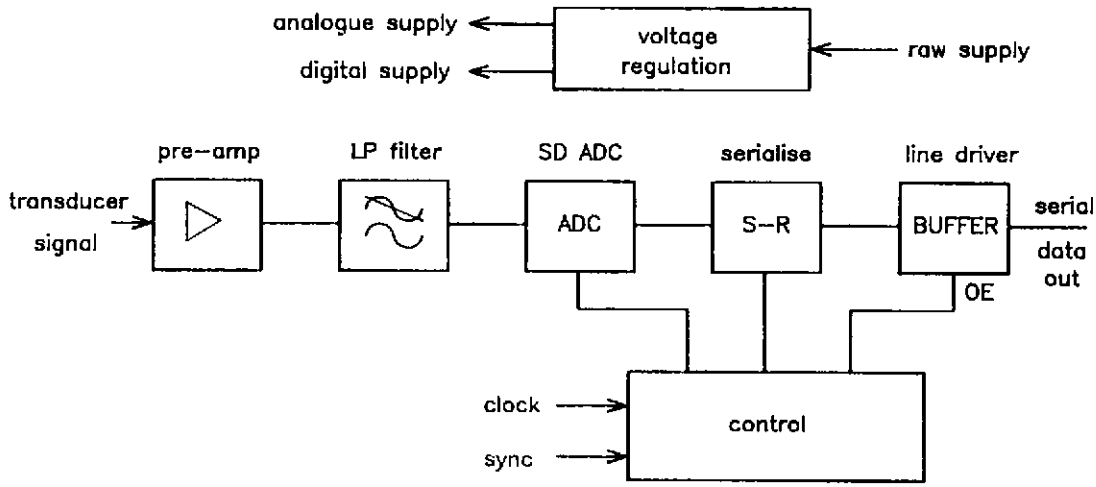

Figure 9 - Complete signal aquisition system schematic.

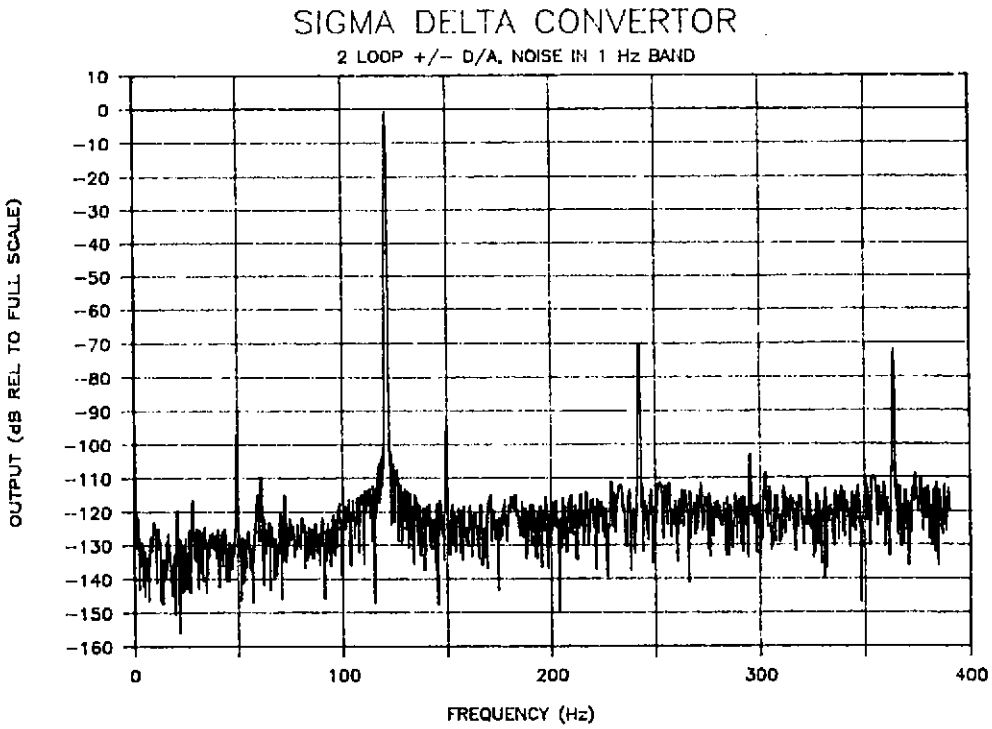

Figure 11(a) - ADC output spectrum for full scale input signal. (note noise background level limited by source)

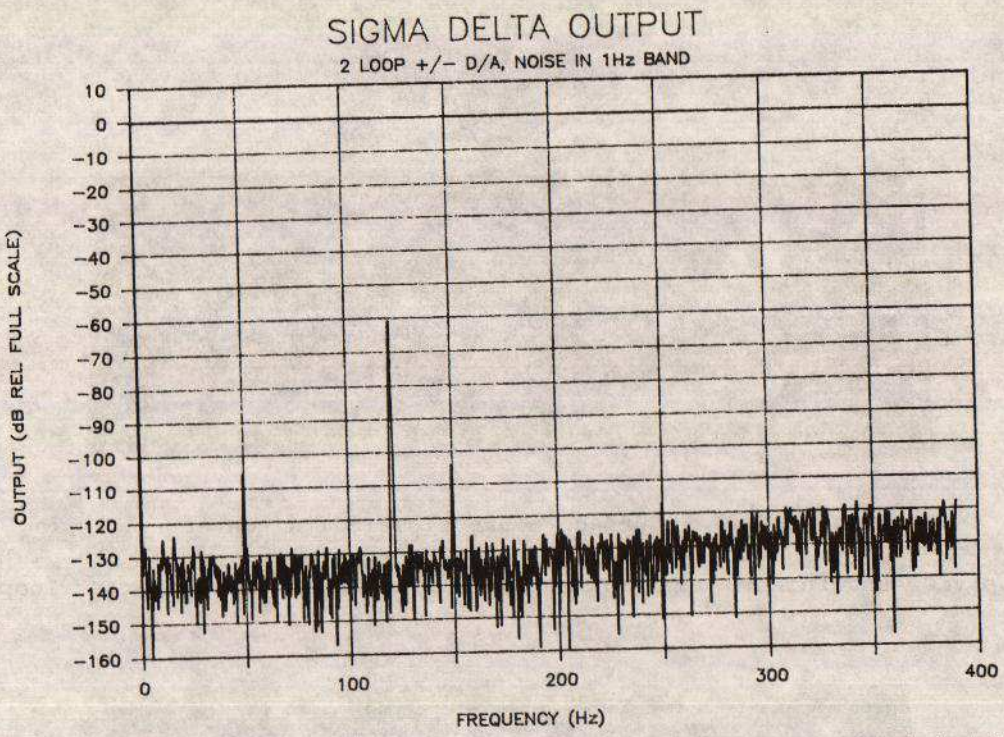

Figure 11(b) - ADC output spectrum for input signal level 60dB below full scale.

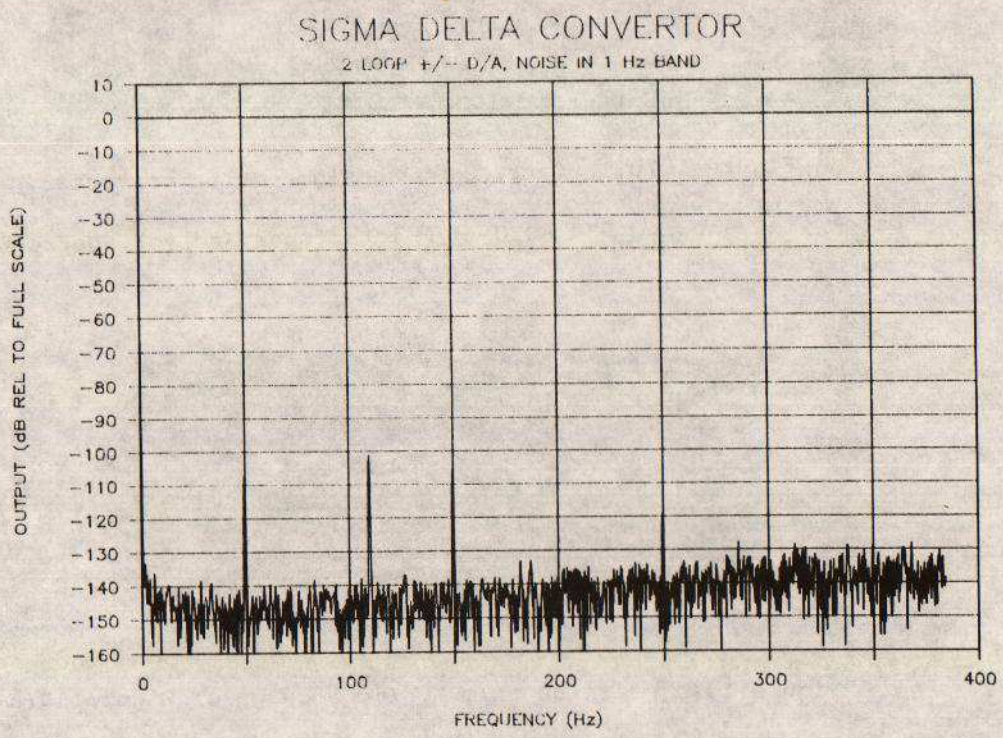

Figure 11(c) - ADC output spectrum for input signal level 100dB below full scale.

HIGH PERFORMANCE SIGNAL ACQUISITION SYSTEMS FOR SONAR APPLICATIONS

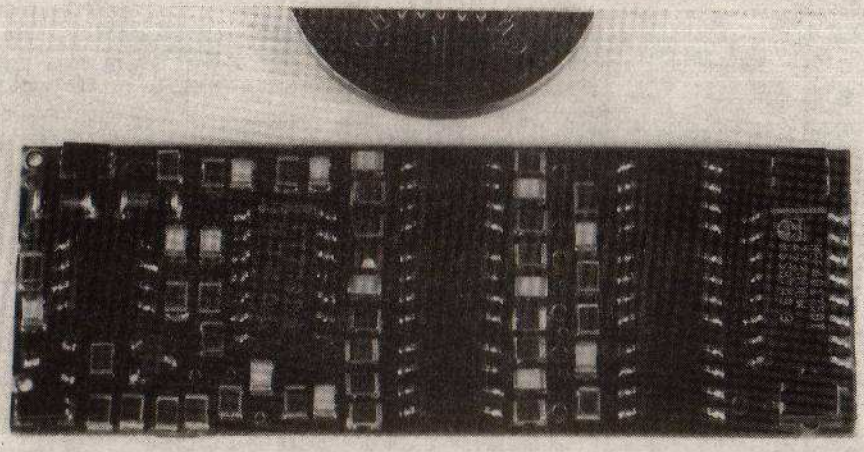

Figure 10(a) - Surface mount sigma-delta converter.

Top view showing pre-amp, anti-alias filter and three converter loops.

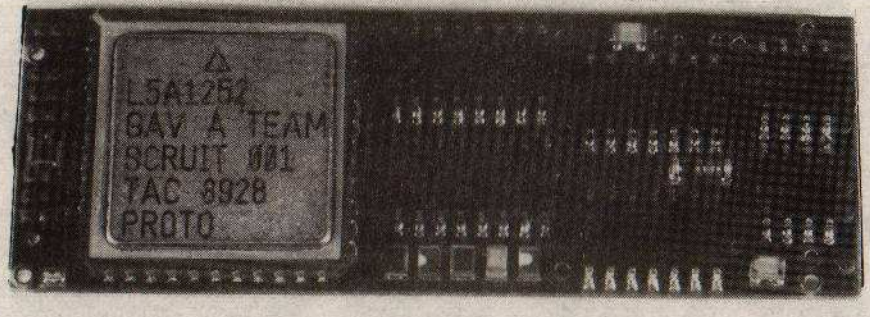

Figure 10(b) - Surface mount sigma-delta converter.

Bottom view showing DSP ASIC, I/O interfaces and voltage regulators.

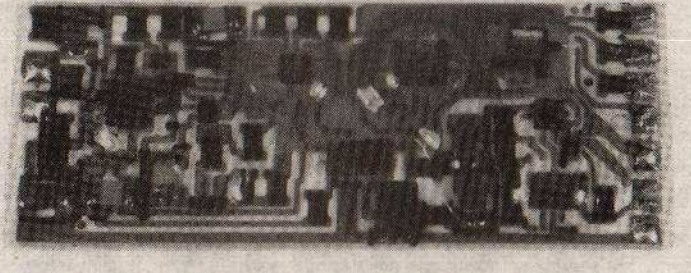

Figure 10(c) - Thick film hybrid version of Figure 10(a).